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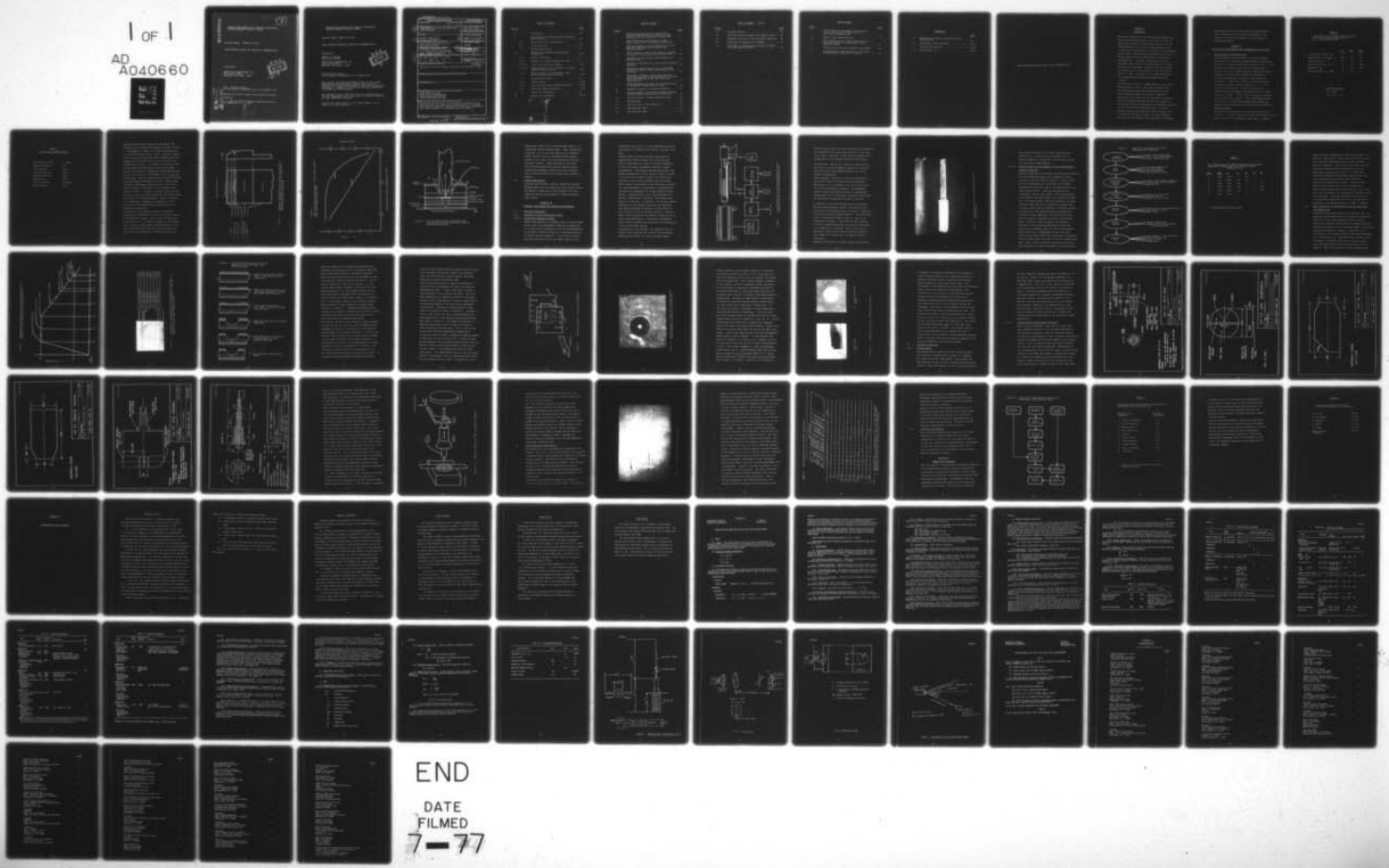

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MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING
PROGRAM QUARTERLY TECHNICAL REPORT

Contract Number DAAB07-76-C-8135

LIGHT EMITTING DIODES FOR FIBER OPTIC COMMUNICATIONS

Prepared By:

LASER DIODE LABORATORIES, INC.
205 Forrest Street
Metuchen, New Jersey 08840

First Quarterly Report
For the Period 30 September 1976 to 31 December 1976

Approved for public release; distribution unlimited.

Placed by:

U. S. Army Electronics Command, Production Division
Fort Monmouth, N. J. 07703

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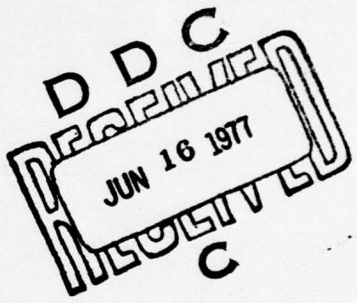

First Quarterly Report
for the Period 30 September to 31 December 1976

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The design and fabrication of high speed etched-well light emitting diodes for fiber optic communications is discussed with regard to materials synthesis via LPE, wafer fabrication, and device assembly in a manufacturing environment.

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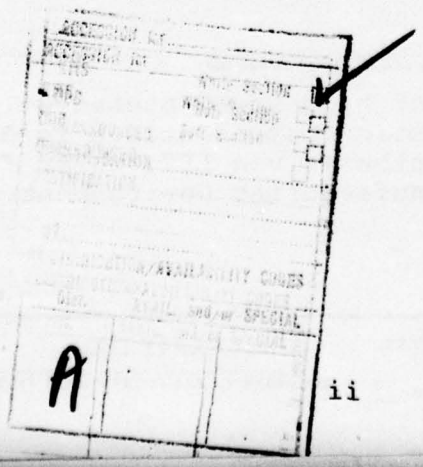
TABLE OF CONTENTS



LIST OF FIGURES

LIST OF FIGURES (Cont'd)

LIST OF TABLES

APPENDICES

Light Emitting Diodes for Fiber Optic Communications

SECTION I

INTRODUCTION

The primary objective of this Manufacturing Methods and Technology Engineering Program is twofold. First, the manufacturing methods and techniques necessary for the volume production of the light emitting diode for use in fiber optic communications as outlined in Specification SCS-511 must be developed and implemented to insure the highest degree of device quality and reliability at a reasonable cost. Secondly, verification of device performance and quality for LED's produced in a volume manufacturing environment must be carried out by means of rigorous testing and evaluation in accordance with SCS-511 in order to demonstrate the technical adequacy of the manufacturing methods developed under this contract.

With this goal in mind, the MMTE program for the Light Emitting Diode for Use in Fiber Optic Communications was organized utilizing the Program Evaluation and Review Technique (PERT) for planning, scheduling, controlling, and evaluating the progress of the program. The major program objectives for the first quarter of the program include the procurement of components essential for the fabrication of prototype LED's, preliminary evaluation of epitaxial material, and the construction of life racks and test fixtures to be used throughout the course of the program. The procurement of materials

and equipment along with the status of process development of manufacturing techniques is discussed in the following sections with respect to the achievement of program milestones.

SECTION II

DEVICE DESIGN REQUIREMENTS AND PERFORMANCE SPECIFICATIONS

2.1 Electro-Optical Characteristics.

The performance characteristics of the Light Emitting Diode for Use in Fiber Optic Communications are described in detail in Technical Specification SCS-511 (App. C). The device may be generally described as a double-heterojunction (DH) GaAs - GaAlAs etched well incoherent emitter capable of high data rate transmission optimized for an emitting wavelength of 820 nm at room temperature. In addition, a fiber optic pigtail is incorporated into the device in order to permit coupling to the optical link via fiber splicing. An outline of the major electro-optical performance characteristics of the device is shown in Table 1. Table 2 lists the optical characteristics of the fiber pigtail. A more detailed description of the device, including environmental performance and parameter test methods can be found in SCS-511 (Appendix C).

2.2 Device Structure

To achieve the electro-optical characteristics outlined in Table 1, a double heterojunction (DH), GaAs-GaAlAs structure having a very thick transparent window layer is employed.

TABLE 1.

Electro-Optical Performance Characteristics of the Light Emitting Diode for Use in Fiber Optic Communications.

	Min.	Max.	Units
Optical Output Power, P_{opt}	0.5	-	mW
Peak Emission Wavelength, λ_p	800	830	nm
Spectral Width, $\Delta\lambda$	40	45	nm
Rise and Fall Time, t_r, t_f	10	20	nsec
Bandwidth, B_{Hz}	32	44	MHz
Forward Voltage, V_f @ 20mA	-	1.9	V

Operating Condition

I_F = 100mA

Ta = 25°C $\pm$ 5°C

TABLE 2.

OPTICAL FIBER CHARACTERISTICS

Attenuation @ 820nm	45 db/Km
Numerical Aperture	0.3
Core Diameter	120μm
Cladding Diameter	150μm
Sheathing Material	Teflon
Sheathing O.D.	.040"
Tensile Strength	55 Newtons
Bending Radius	.060"

Details of the epitaxial structure required for the production of the etched well emitter are shown in Figure 1. The substrate, region 1, is n-type GaAs doped with Si to $2x10^{18}/cm^3$ with an EPD < $1K/cm^2$. Region 2 consists of an n-type $Ga_{.7}Al_{.3}As$ window layer through which light generated by the injection of carriers into the lower bandgap active region 3, is coupled to the optical fiber. The low absorption coefficient of the n-type GaAlAs window layer renders it transparent to the 820nm emission from the active region. The bandgap of the $Ga_{.94}Al_{.06}AS$ active region, hence the aluminum concentration, determines the peak emission wavelength of the LED. Maximum power efficiency and minimum risetime occur when the active region is doped $\simeq 1x10^{18}$ with Ge as indicated by the curves in Figure 2. Region 4, a p-type $Ga_{.7}Al_{.3}As$ layer, serves to confine carriers injected into the active region by virtue of its increased bandgap. Region 5 functions as a contact cap. Aluminum is incorporated in this p-type layer to minimize lateral current flow by increasing its resistivity.

The diameter of the emitting surface is determined primarily by the diameter of the circular contact applied to the surface of region 5 and the sheet resistivities of regions 4 and 5. As shown in Figure 3 by the dashed lines, current is restricted to flow through the active region directly under the circular aperture which has been selectively metallized. To facilitate selective

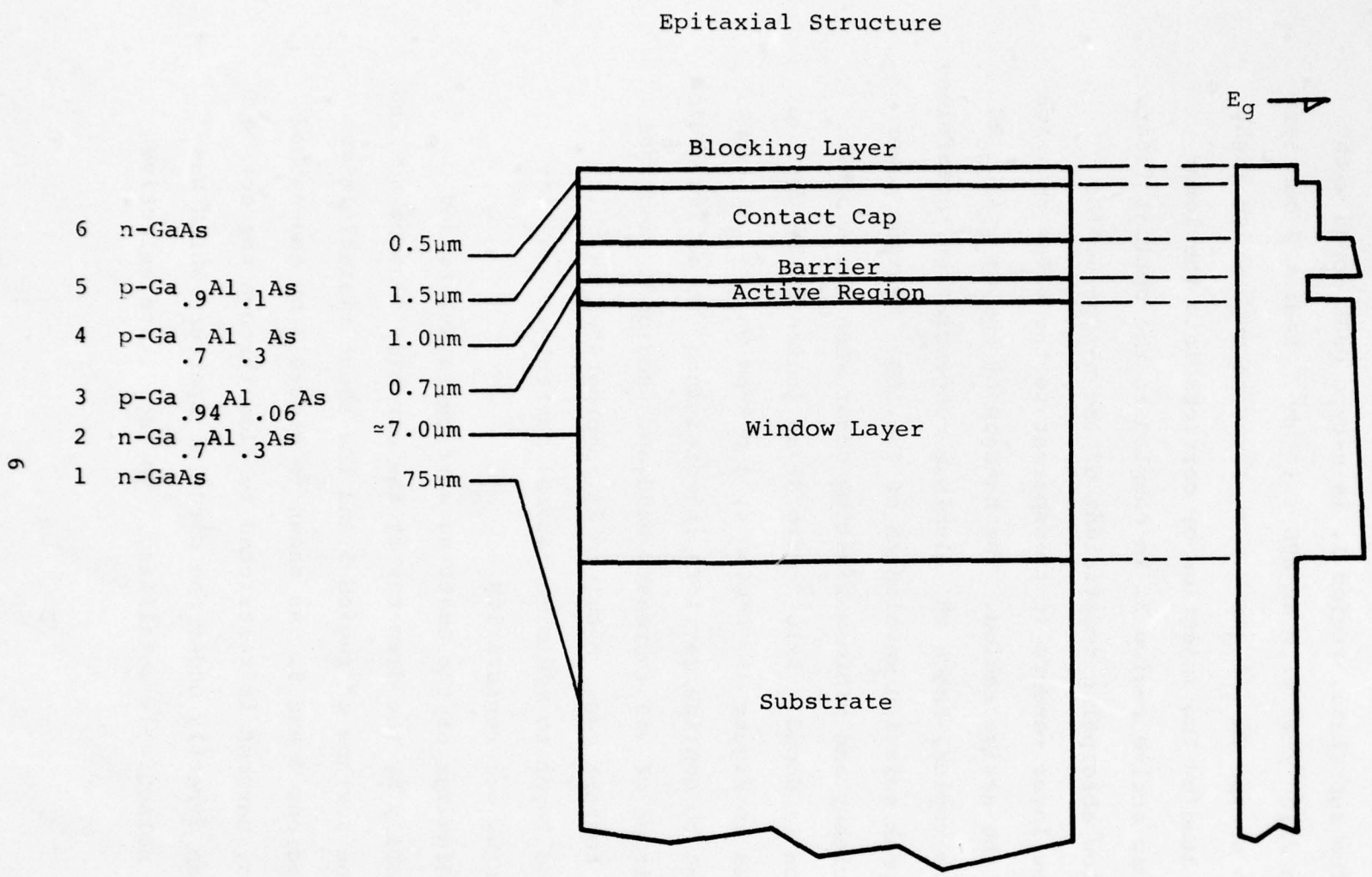
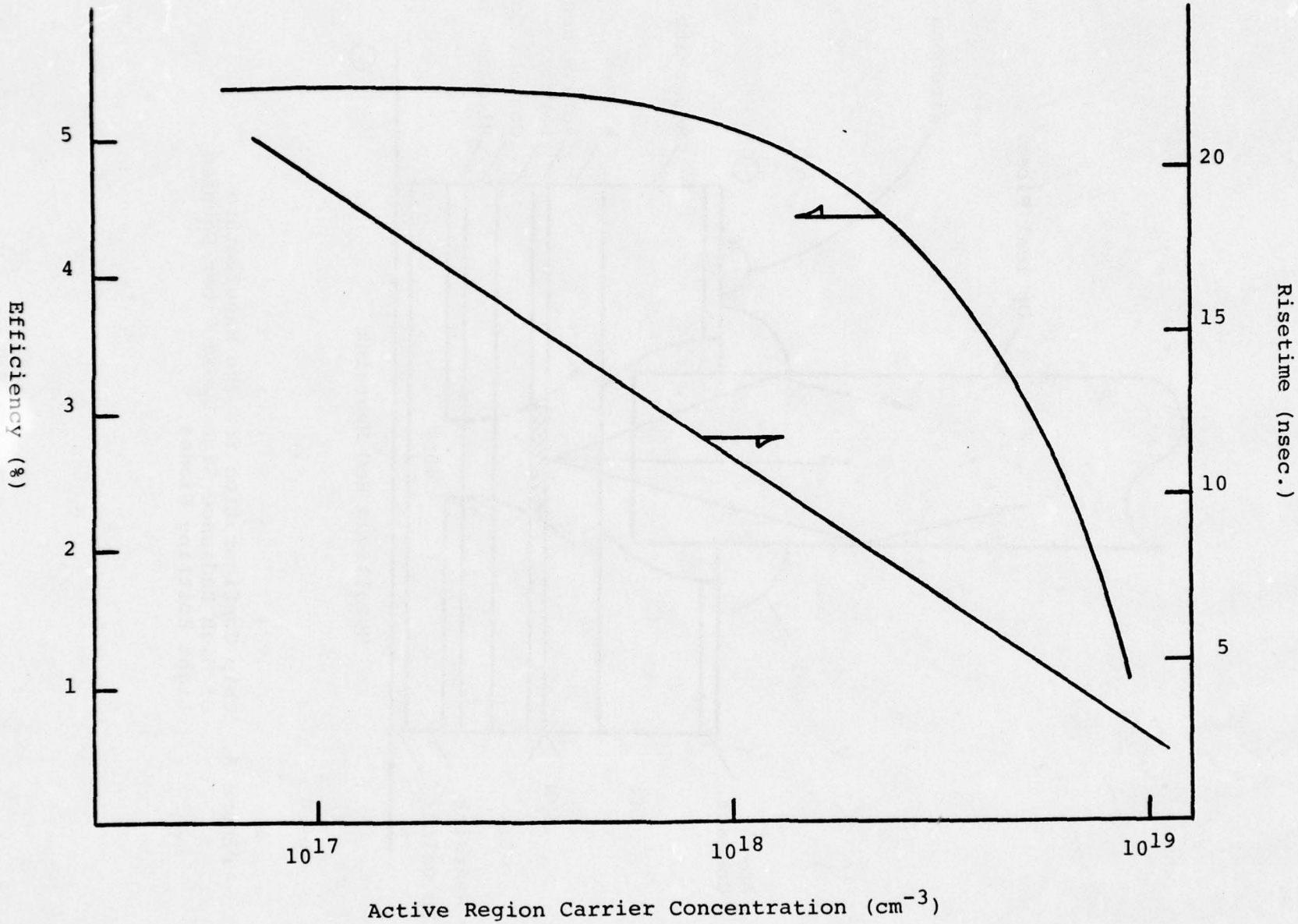


Figure 1. Schematic Representation of Double Heterojunction Epitaxial Structure for Use in the Fabrication of the Fiber Optic Coupled LED.

Figure 2.

Power Efficiency and Risetime vs. Active Region Doping Level for Germanium Doped LEDS.



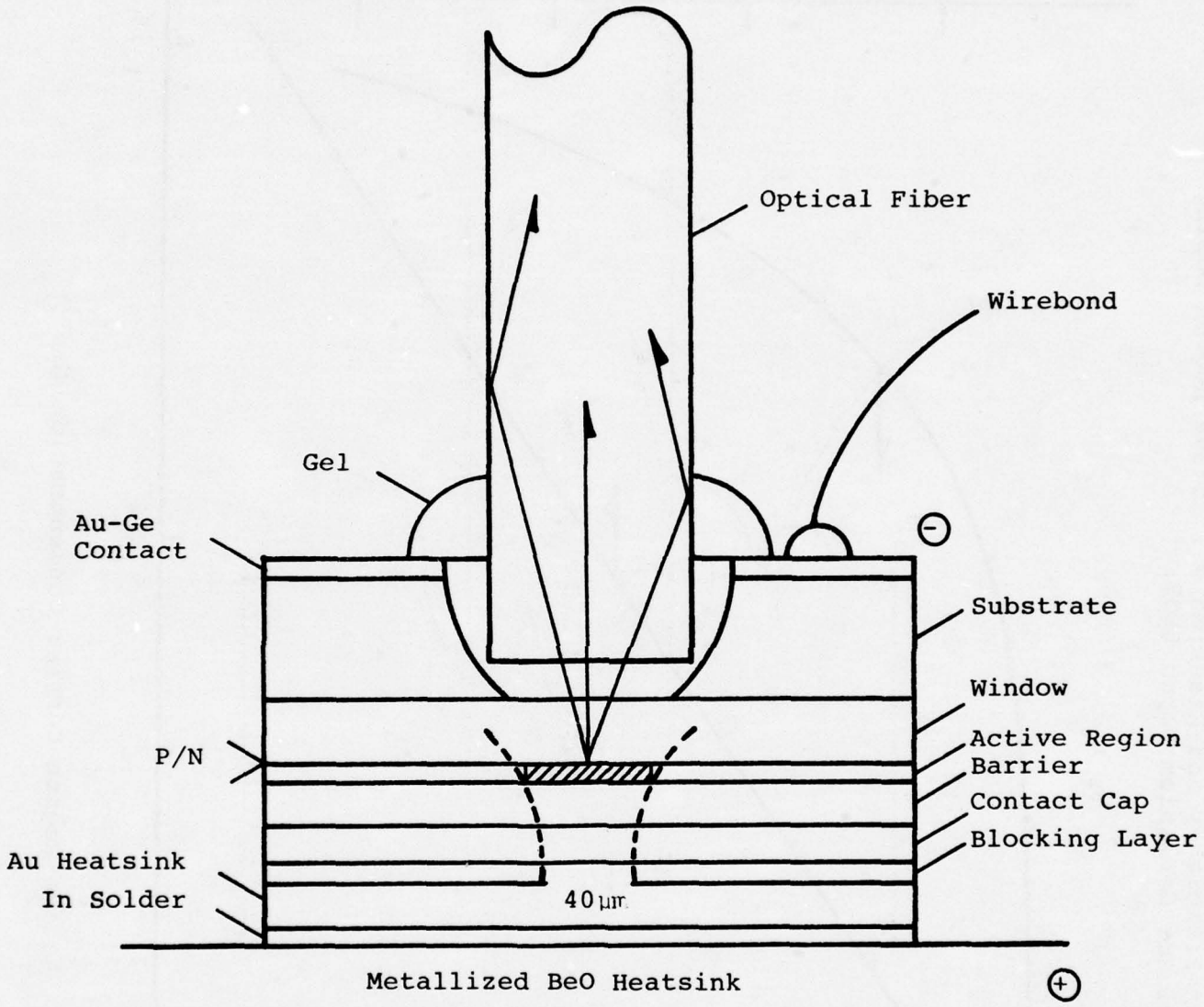


Figure 3. Chip Configuration for the Manufacture of High Radiance High Speed Fiber Coupled Light Emitting Diodes.

contacting, a 40μm hole is etched through region 6, an n-type GaAs current blocking layer. Under forward bias conditions, the P-N junction formed at the interface between region 5 and 6 is reversed biased allowing current to flow only in the region directly below the 40μm ohmic contact. Light generated in the active region directly above this circular aperture passes through the transparent window layer and is emitted from the bottom surface of the etched well as shown in Figure 3.

2.3 Package Requirements

Technical Specification, SCS-511, defines the outline package drawing for the etched well light emitting diode. The package is based upon a dual stripline stud configuration and has been modified to accept an optical fiber pigtail.

SECTION III

MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING

3.1 Materials Technology.

3.1.1 Synthesis of Device Structure via LPE.

3.1.1.1 Liquid Phase Epitaxial System.

Liquid phase epitaxy is a complex process in which single crystal layers of semiconductor material are deposited on a single crystal substrate of lattice matched material by precisely controlled cooling of a saturated solution in contact with the substrate. In the case of hetero-epitaxial synthesis of GaAs and GaAlAs layers for LED

fabrication, gallium (Ga) is the preferred solvent and the substrate is normally high quality, low EPD, (100) GaAs.

Crystal growth of these structures takes place at temperatures ranging between 750°C and 900°C and must be performed in an inert or reducing atmosphere to avoid the highly detrimental effects of oxygen contamination. The properly designed LPE reactor and support systems must satisfy several criteria in order to yield epitaxial wafers suitable for fabricating monolithic triple stripe geometry laser structures. These criteria are dictated by the uniformity, reliability, and produceability requirements of semiconductor optoelectronic components for volume commercial manufacture. Maximum surface area, layer thickness uniformity, compositional uniformity, and minimum defect density are required. In addition, the as-grown surface morphology of the terminal layer must be compatible with photolithographic processing for the definition and patterning of stripe geometry contacts. Figure 4 shows a block diagram of the epitaxial system in use at Laser Diode Laboratories. This system incorporates several features which have resulted in the optimization of the liquid phase process:

Isothermal Heat Pipe Furnace: The sodium filled isothermal liner eliminates all vertical and horizontal temperature gradients and, hence provides uniform

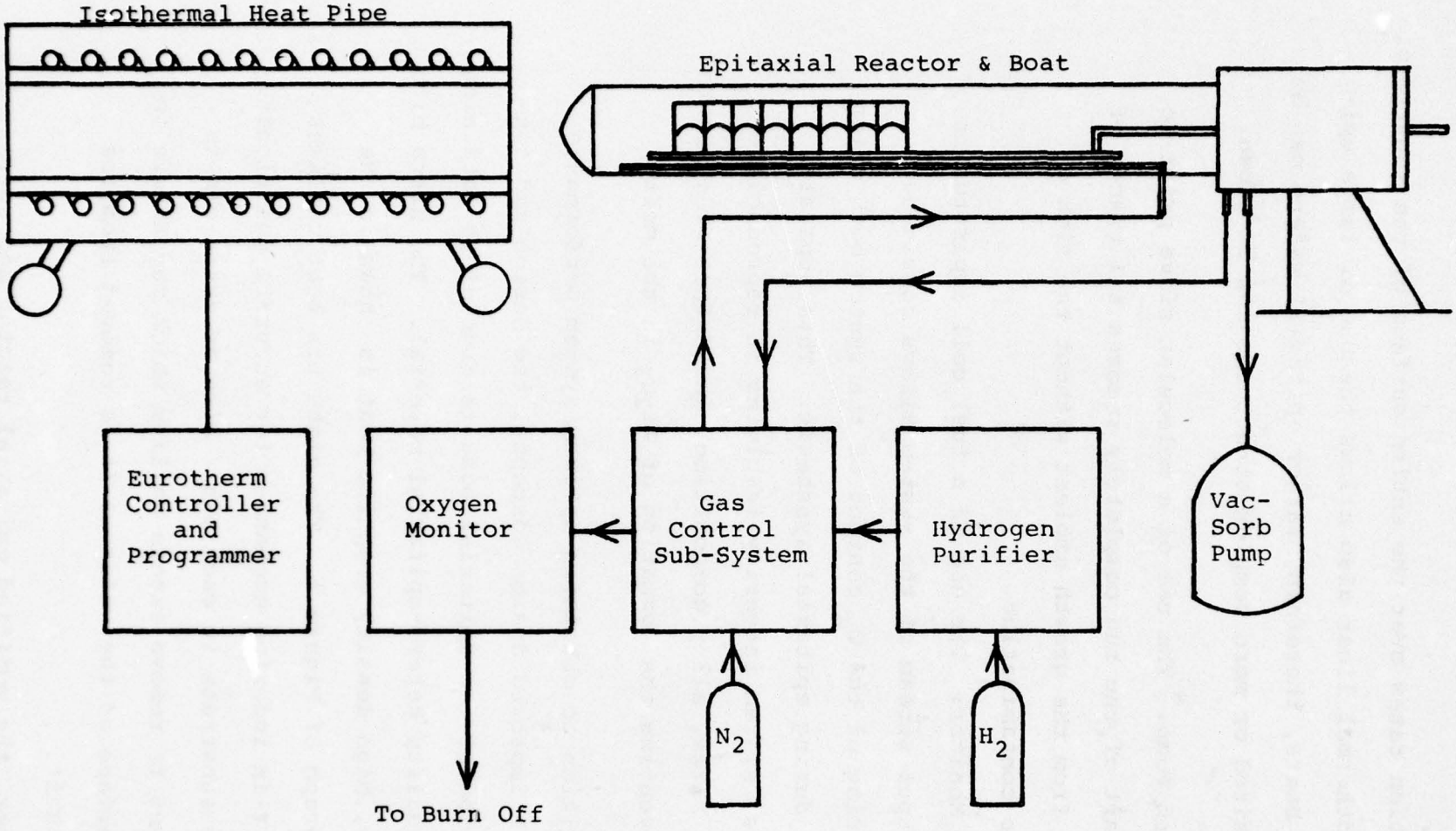


Figure 4. Block Diagram of Liquid Phase Epitaxial Systems Currently in Use at Laser Diode Laboratories.

deposition rates over the entire surface of the substrate. The isothermal liner also allows the use of large epitaxial boats, therefore, larger epitaxial wafers can be synthesized or more complex structures can be grown.

Vac Sorb Pump: The use of a molecular sieve prior to the start of the run completely removes all traces of oxygen from the growth ambient without the risk of organic contamination.

Oxygen Monitor: The use of a fuel cell apparatus in the output stream of the system allows continuous monitoring of the O_2 content of the system both prior to and during epitaxial synthesis. This apparatus assures system integrity resulting in reproducible growth rates, alloy composition, and defect free growth by preventing the formation of Al_2O_3 in the melt.

In addition to obtaining optimum system performance through improved design concepts, the design and construction of the epitaxial boat is crucial to obtaining high quality hetero-epitaxial material. The ultra high purity, high density graphite boat is shown in the photograph of Figure 5. The eight bin boat utilizes a built-in indexing mechanism for accurate positioning of the substrate in each bin. Also an extra bin is employed to remove excess gallium which may adhere to the surface of the wafer as it is removed from the final melt.

Together, the modified epitaxial reactor and epitaxial

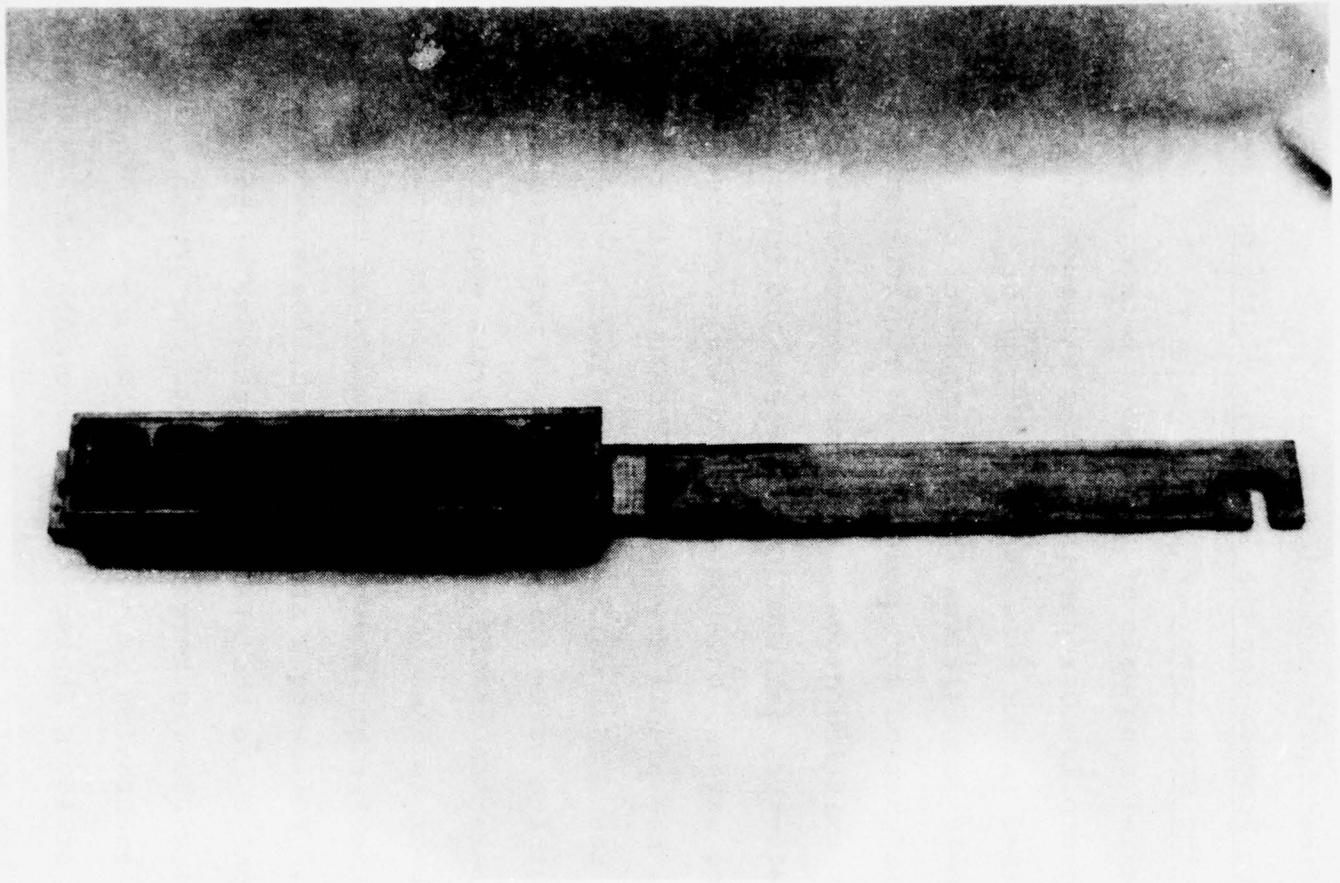


Figure 5. Photograph of High Purity Graphite Multi-bin Epitaxial Boat.

boat allow the generation of double heterojunction structures in a manufacturing environment for the volume production of etched well light emitting diodes for fiber optic communications.

3.1.1.2 Growth Process for the Synthesis of the Double Heterojunction Structure.

Epitaxial synthesis of the double heterojunction structure is accomplished according to the sequence of events outlined in the flow chart of Figure 6. Table 3 lists the melt compositions for the growth of the double heterojunction structure used in the fabrication of the light emitting diode. After the appropriate melt ingredients, gallium (Ga) charges, and polycrystalline source wafers, have been loaded into consecutive growth bins, the single crystal (100) GaAs substrate is placed into the slider well of the high purity graphite boat. A graphite cover plate is employed to eliminate surface dissociation of the substrate during equilibration. The boat is then loaded into the quartz growth tube and the system is evacuated by means of the Vac-Sorb pump. Following a short H_2 purge, the system is brought up to the starting temperature of 850°C by rolling the isothermal liner into the growth position. Melt saturation is accomplished during a one hour soak at 850°C during which time enough GaAs is dissolved from the source wafers in order to exactly saturate each melt. This recently developed self-saturation scheme has simplified the growth procedure by eliminating the

Figure 6. Sequence of Operations for Liquid Phase Epitaxial Synthesis.

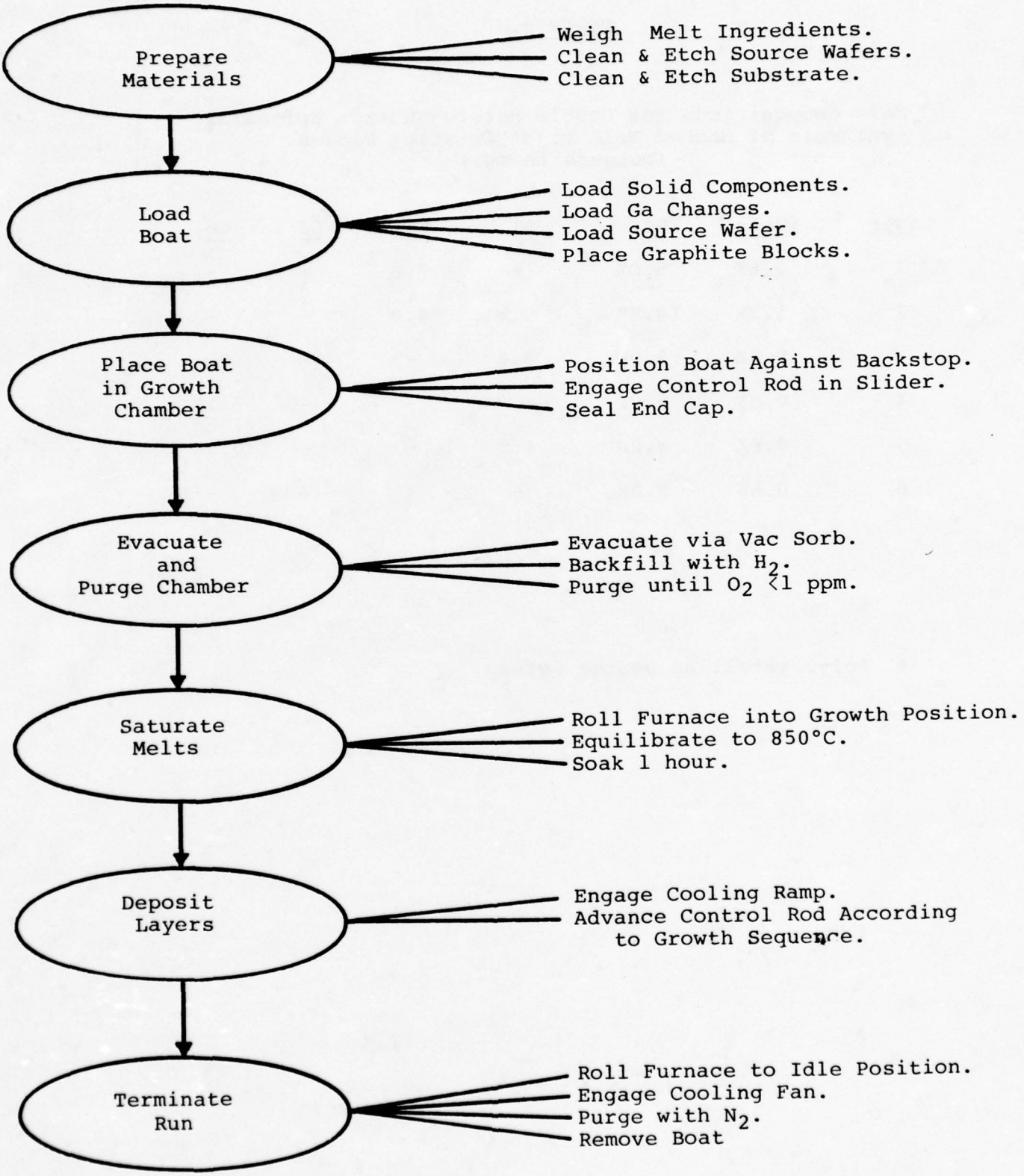


TABLE 3.

Melt Compositions for Double Heterojunction Epitaxial Synthesis of Etched Well Light Emitting Diodes.
(Weights in mg.)

Layer	*GaAs	Ga	Al	Te	Si	Ge
1	0.6K	5.OK	-	2.0	-	-
2	1.2K	10.0K	9.0	4.0	-	-
3	0.6K	5.0K	0.8	-	-	20
4	0.6K	5.0K	6.0	-	-	0.1K
5	0.6K	5.0K	1.2	-	-	0.5K
6	0.6K	5.0K	-	-	-	-

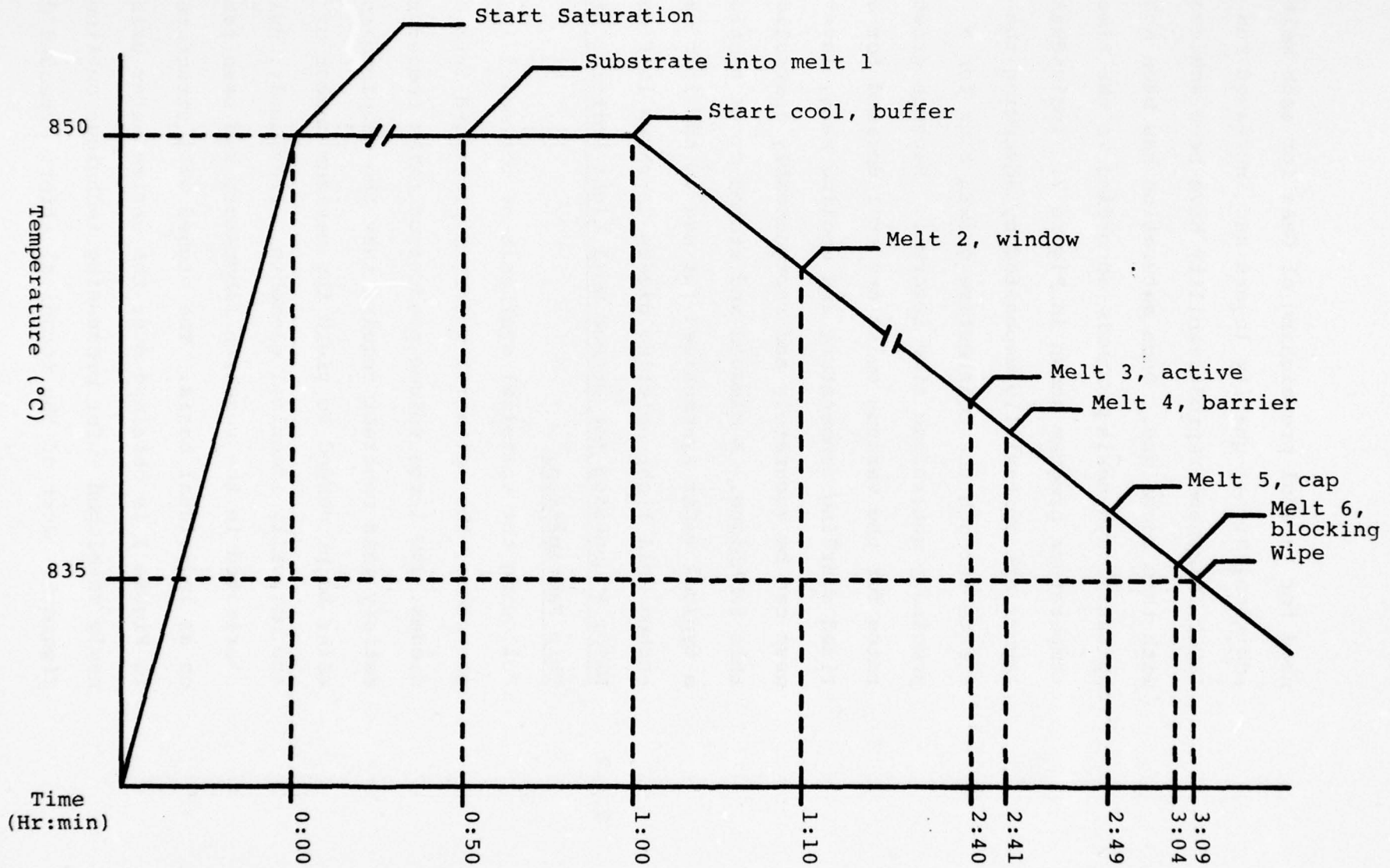
* Polycrystalline source wafers.

need for careful preweighing of GaAs for each melt. In addition, higher quality layers and increased run to run layer thickness reproduceability have been achieved with this technique. Once saturation has been achieved, epitaxial synthesis proceeds according to the time temperature program shown in Figure 7. Individual layers are epitaxially deposited by advancing the substrate through the consecutive growth bins for a precisely controlled time interval. Because growth rates for the various melts are well defined for a fixed starting temperature and cooling rate, layer thickness can be accurately and reproduceably controlled using this technique. A cleaved and etched cross section of a typical wafer synthesized for use in the fabrication etched well light emitting diodes is shown in Figure 8.

3.1.2 Wafer Processing for Etched Well Light Emitting Diode Chip Fabrication.

Following the epitaxial synthesis of the multi layer DH structure, the epitaxial wafer is processed into discrete diodes. The large volume production rates needed to satisfy this contract require that the complete epitaxial wafer be processed to yield the maximum number of physically and optically identical elements. Previously, units fabricated in the research laboratory had been fabricated on an individual basis. The etched well structure shown in Figure 3 is obtained over the entire wafer using a newly developed wafer processing technique outlined in Figure 9. Most of the technical effort expended during

Figure 7. Temperature Program Used in the Liquid Phase Epitaxial Growth of Double Heterojunction LED Structures.



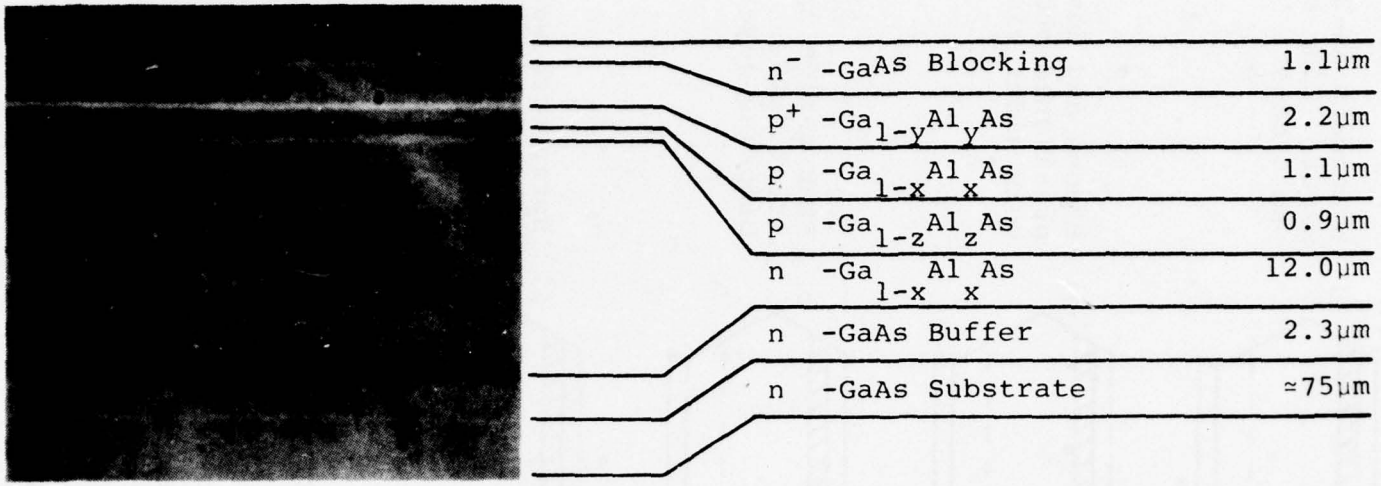
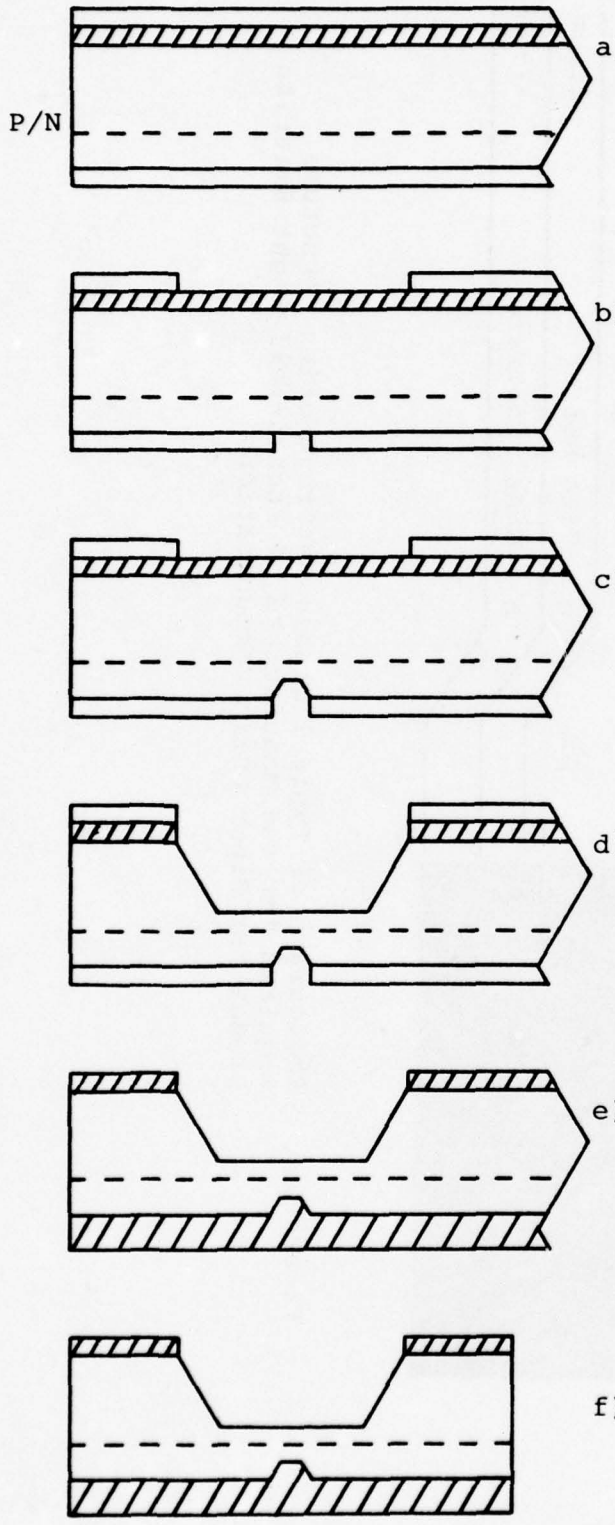


Figure 8. Photograph of Typical Double Heterojunction Structure Required for the Manufacture of Etched-Well Light Emitting Diodes for Fiber Optic Communications.

Figure 9. Wafer Processing Flow Chart for the Manufacture of Etched-Well Light Emitting Diodes.



a) Evaporate Au-Ge onto n-side of wafer. Coat both sides with photoresist.

b) Expose and develop resist using prealigned photomask to expose both sides simultaneously.

c) Etch p-side aperture with 3:1:1 H_2PO_3: H_2O_2:H_2O through blocking layer.

d) Spray etch well with pH adjusted NH_3OH:H_2O_2.

e) Strip resist and electroplate p-side of wafer to form integral heat sink.

f) Wire saw wafer into discrete diodes.

the first quarter of the program has been devoted to optimizing and simplifying what is normally considered to be an extremely difficult and complex procedure. There are three major obstacles to be overcome in order to obtain the structure outlined in Figure 3. In the order of difficulty, they are as follows: a) the 'blind' front-to-back alignment of the fiber well and emitting aperture; b) the accurate control of the fiber well depth to guarantee that the bottom of the well intersects the window layer (region 2 in Figure 1); and c) the accurate control of the emitting aperture depth necessary to punch through the blocking layer (region 6 in Figure 1). Secondary problems involving the ability to maintain circularity as the well is being etched and the ability to control the slope of the walls also had to be addressed and solved.

The original approach to the solution of these problems involved the use of a two step 'blind' alignment which depended on critical mask alignment with two mutually perpendicular <110> cleavage reference. In theory, this technique should render perfect front-to-back alignment of the etched fiber well to the contact aperture. It was determined, however, that a misalignment of several hundredths of degree could result in as much as a 50% reduction in device yield due to nonconcentricity of the emitting aperture beneath the etched fiber well. In the newly developed processing technique outlined in

Figure 9, this problem has been solved by using a single step alignment in which both sides of the epitaxial wafer are simultaneously exposed through a specially designed pre-aligned photoresist mask.

After the epitaxial wafer is grown and inspected to determine layer thicknesses, the wafer is thinned to approximately .005". A thick (5μm) layer of Au-Ge is then deposited on the n-side of the wafer. The thick metal deposition, in addition to serving as the ohmic contact to the n-type material, resists undercutting of the unexposed regions of the wafer during subsequent etching steps. Photoresist is then applied to both sides of the wafer as shown in Figure 9(a). Following a 30 min. curing step, the wafer is placed between the prealigned plates of the specially designed photoresist mask shown in Figure 10. The plates are attached to a flexible hinge which serves to clamp the epitaxial wafer between the masking plates. Both n- and p-sides of the wafer are then simultaneously subjected to ultraviolet light in order to expose the unmasked regions of the wafer as shown in Figure 9(b). Figure 11 shows photomicrographs of the prealigned mask with the emitting pattern clearly visible and accurately centered within the well pattern. The diameters are 40μm and 225μm respectively. The exposed photoresist is then developed leaving a 40μm diameter area of exposed GaAs and a 225μm area of exposed Au-Ge over GaAs. In Figure 9(c), the

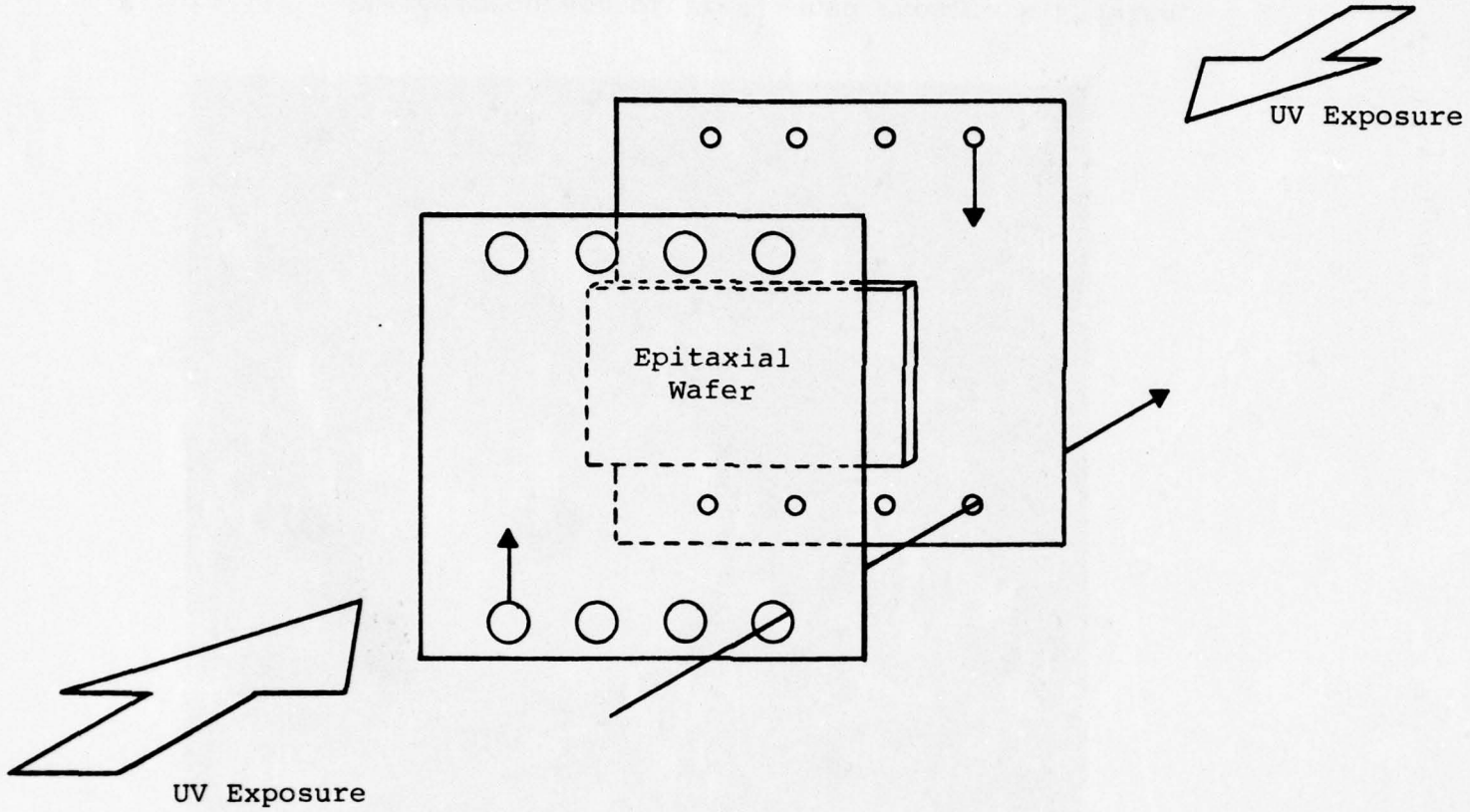


Figure 10. Schematic Diagram of Prealigned Photomask.

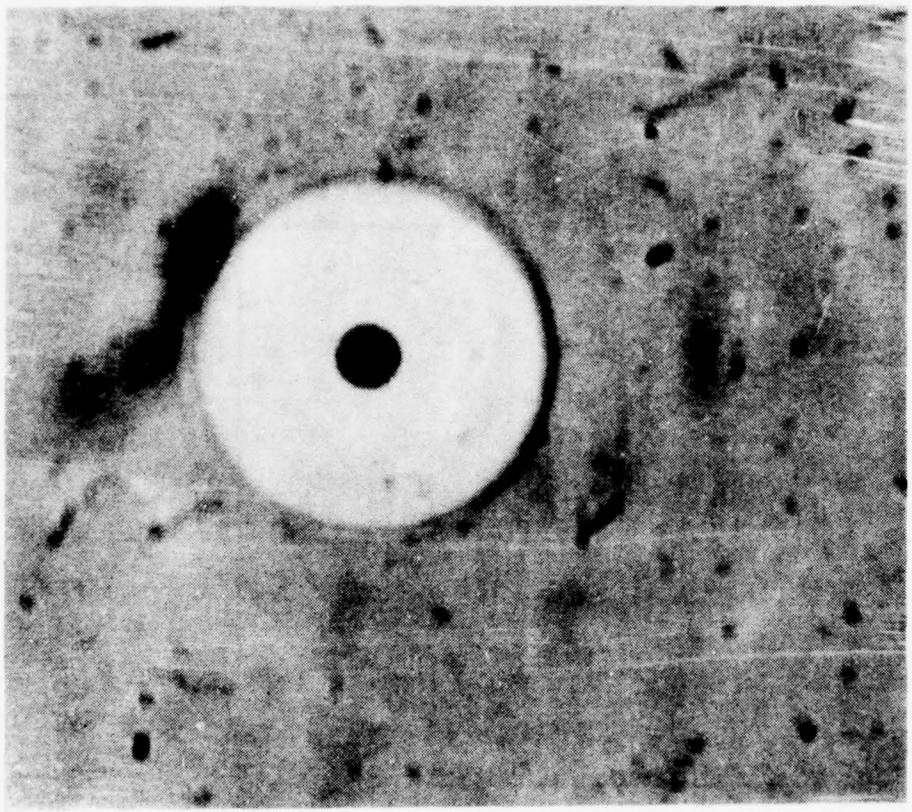
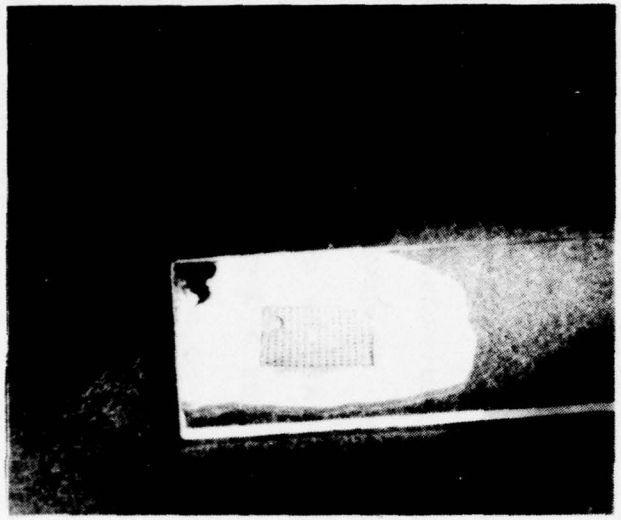
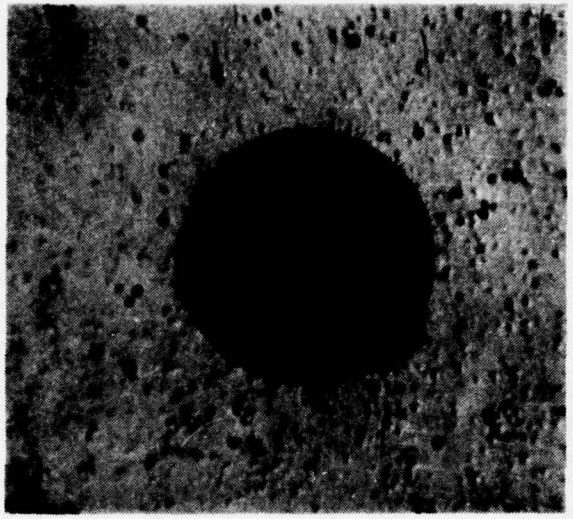


Figure 11. Photomicrograph of Prealigned Photomask Showing Contact Aperture Centered in the Fiber Well.

emitter aperture (p-side contact aperture) is opened up by carefully etching the wafer in 3:1:1 H_2PO_3:H_2O_2: H_2O. This etch removes GaAs at a rate of 0.5μm/min. and attacks only the exposed GaAs. After several minutes of exposure to the etchant, the wafer is removed, rinsed, and dried. An interferometer is employed to determine the depth of the contact aperture to insure that punch through to the p-contact layer (region 5 in Figure 1) has been sucessfully accomplished. The wafer is then waxed to a glass slide to protect the completed contact aperture pattern during the well etching step illustrated in Figure 9(d). In this step, the n-side of the wafer is spray etched with a pH controlled solution of NH_3OH:H_2O_2. In this process, the 9 mil circular regions of exposed Au-Ge and the n-GaAs beneath these regions are removed at a rate of 2 to 5 μm/min. The photoresist is sufficient to protect the remaining areas of the wafer from attack by the etchant. Figure 12(a) shows the epitaxial wafer after the surface has been spray etched. Figure 12(b) shows an individual well photographed looking down on the top surface. In cross section, the final well diameter is 9.5 mils at the n-surface, 6.0 mils at the bottom of the well, and has a depth of approximately 3.5 mils. The primary advantage to using the NH_3OH:H_2O_2 (stabilized at pH 8.2) results from the fact that the etch does not attack $Ga_{1-x}Al_xAs$ strongly when $x>\sim 0.1$. Hence, when the etched well reaches the n-type $Ga_{1-x}Al_xAs$ window layer (region 2 in Figure 1), the etch rate decreases to



a. Entire Wafer
(X1)



b. Single Etched Well
(X170)

Figure 12. Photomicrographs of Etched Epitaxial Wafer.

<0.2μm/min. By carefully measuring the well depth at fixed intervals during the well definition process, it becomes relatively simple to determine when the well bottom reaches the n-$Ga_{1-x}Al_xAs$ window layer. This measurement is performed accurately by using the focussing index on the Nikon metallurgical microscope. The concentricity and definition of the emitting aperture is then verified by backlighting the wafer with a focussed incandescent beam and observing the bottom of the etched well with an infrared viewer through the microscope. The wafer is then demounted from the glass slide and the photoresist stripped from the wafer. The p-side of the wafer is then electroplated with a thick Au film (~10μm) which functions as an integral heatsink for the individual diodes (see Figure 9(e)). This layer also provides mechanical support for the thin active region of the device. Finally, the epitaxial wafer is cut into discrete LED's using a ganged wire saw. A typical 0.56" x 0.63" epitaxial wafer processed according to the flow chart Figure 9 will produce a maximum of 600 discrete etched-well light emitting diodes.

3.2 Packaging Technology

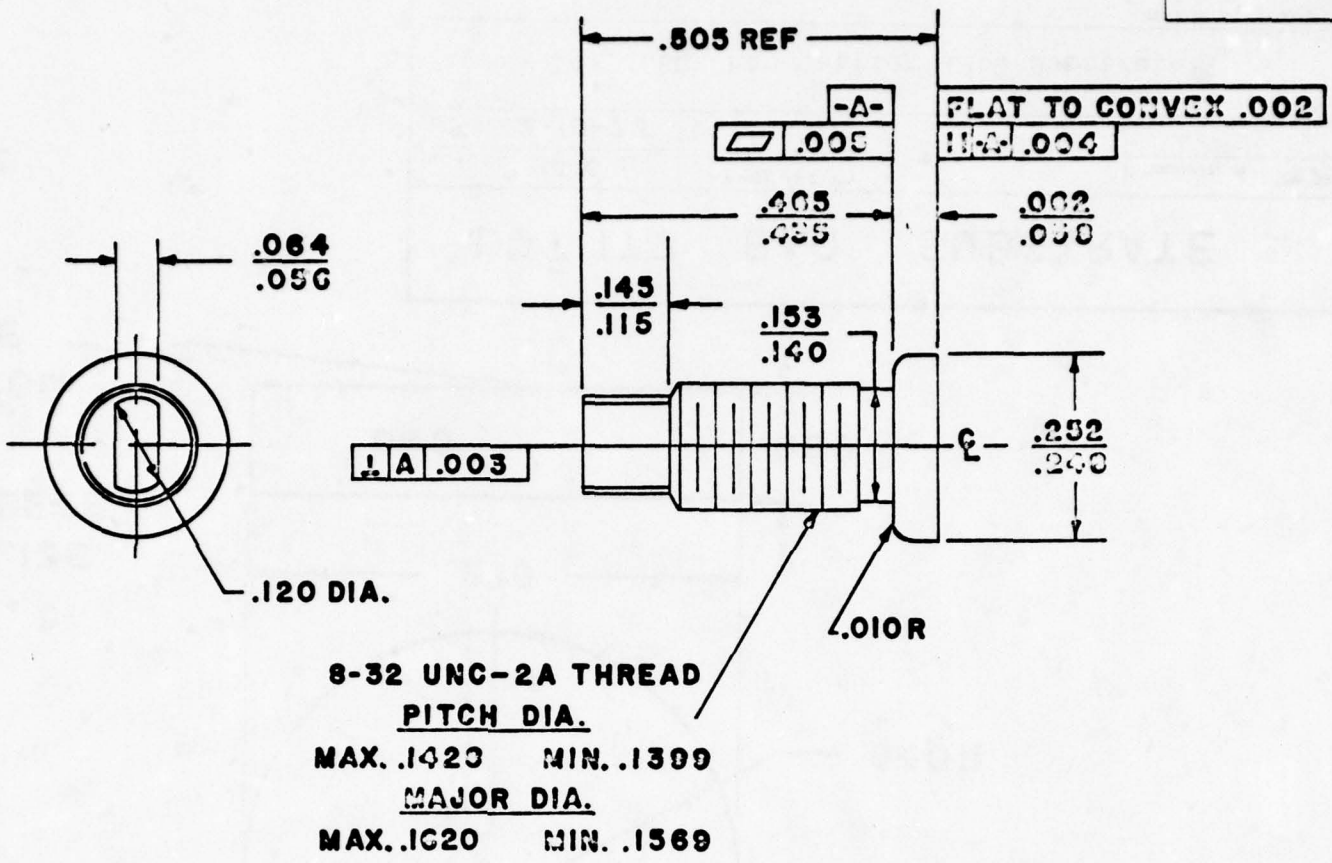
3.2.1 Package Design

The package design used for the light emitting diodes for fiber optic communication is based on a standard RF transistor package (JEDC MT-90). This package has been modified for use with high frequency opto-electronic sources. Piece part drawings for the various elements of

the stud (heatsink) assembly are shown in Figures 13, 14, 15, and 16. Figure 17 is an assembly drawing of the stud base which is being purchased from our supplier as a complete unit. The .020" x .020" LED chip is mounted in the semicircular area in the center of the BeO substrate. The ferrule assembly shown in Figure 18 is also being supplied as a complete subassembly including the fiber pigtail. During the first quarter of the program, pre-production quantities of the stud package were obtained. Because of the somewhat unique fiber characteristic required by SCS-511, procurement of the ferrule assembly has been delayed but a suitable substitution will be incorporated in the engineering sample submissions.

3.2.2 Light Emitting Diode Assembly Technique

Sample lots of etched-well light emitting diodes have been assembled according to the procedure described in the following paragraphs. While the technique appears to function quite adequately, fiber attachment nevertheless remains an extremely delicate and somewhat time consuming process. Prior to mounting, each LED chip is screened for electrical and optical parameters. Measurement of I-V characteristics, near field uniformity, and microscopic examination for dark line defects, is performed by means of a pellet test apparatus specially designed for this purpose. Because the quality of the initial LED lots was relatively poor, acceptance criteria for these tests

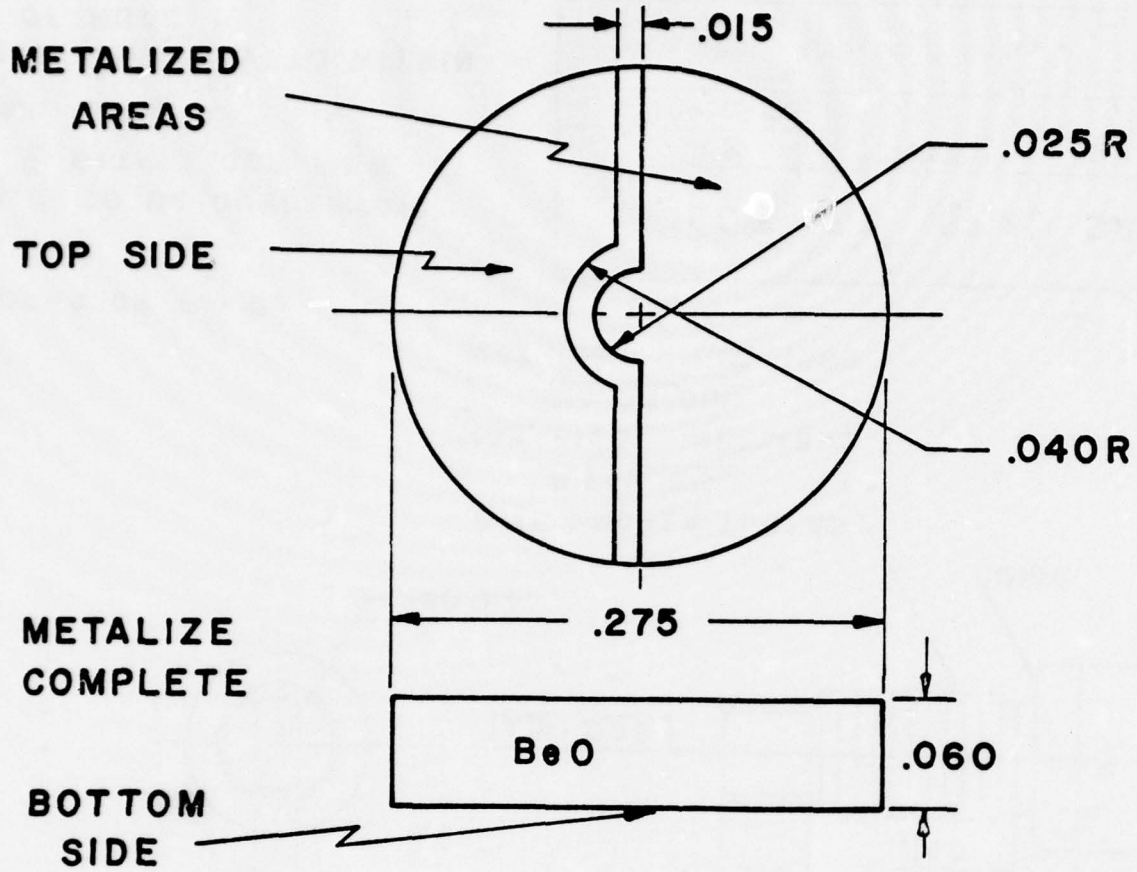


MATERIAL: OFHC OR Te-Cu

NOTES:

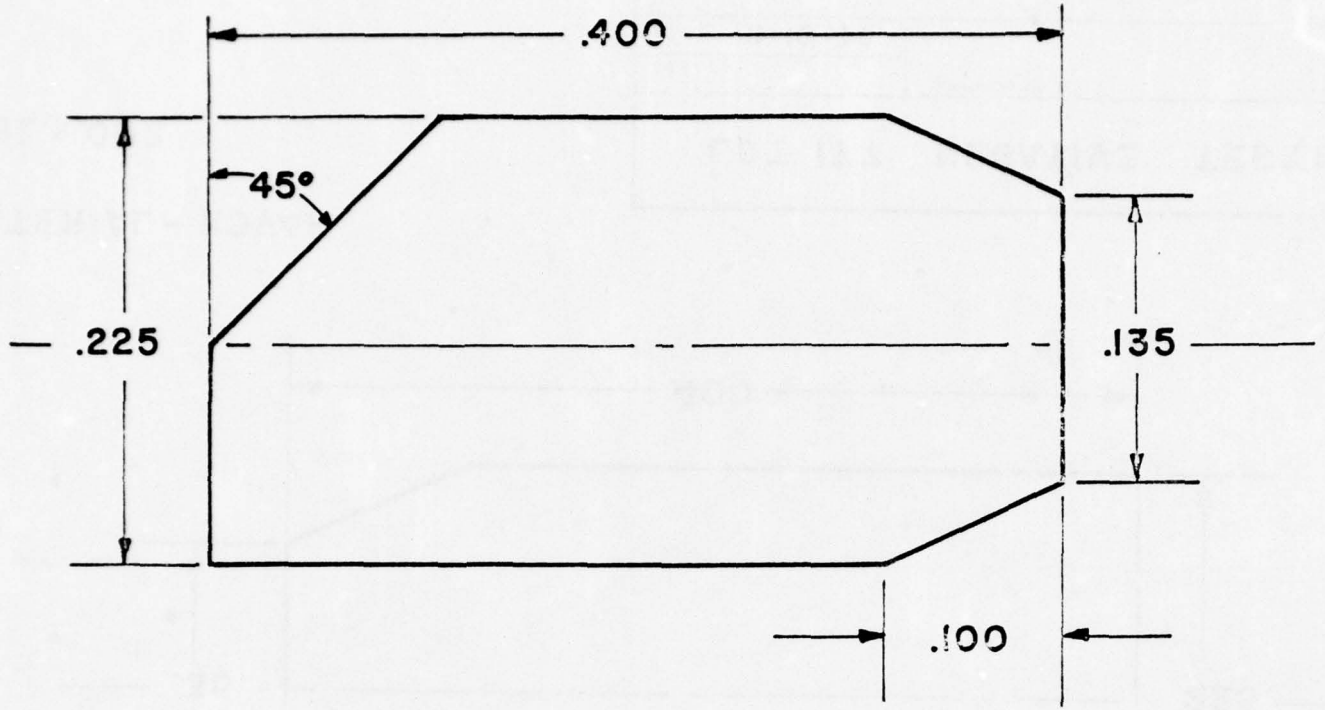
1) ALL DIA,S TO BE CONCENTRIC WITH ℄ WITHIN .005 T.I.R.
2) .002 MAX. BURR
3) COMPLETE THREADS TO WITHIN .040 OF HEAD

LDT 177 STUD BASE		
SCALE: 4X DATE: 12-10-76	APPROVED BY	DRAWN BY M.R.
Figure 13. LED Stud Base.		
LASER DIODE LABS. INC.		DRAWING NUMBER A-40-76



TOL. ± .002

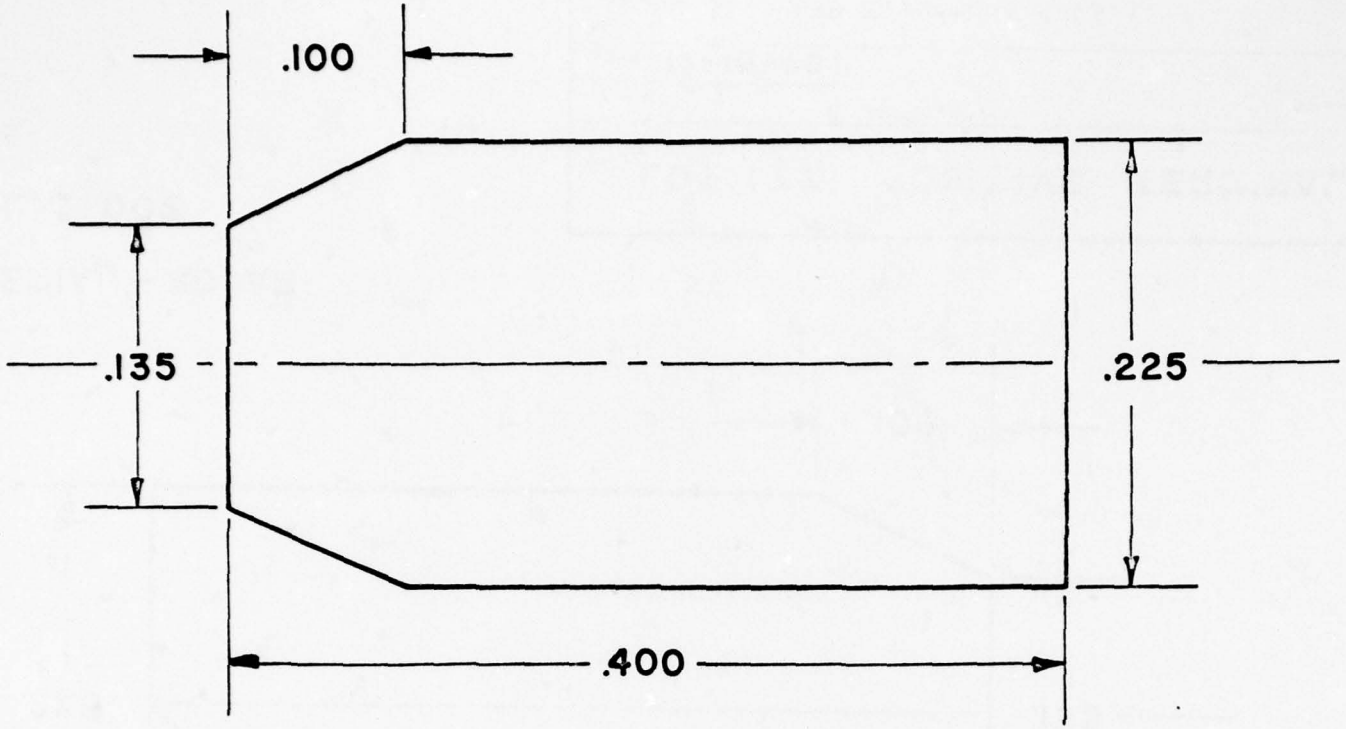
LDT 177 BeO SUBSTRATE		
SCALE: 10X	APPROVED BY	DRAWN BY M.R.
DATE: 12-10-76		
Figure 14. LED Chip Carrier (BeO Substrate).		
LASER DIODE LABS. INC.		DRAWING NUMBER A-00-76



MATERIAL - KOVAR

TOL. ± .002

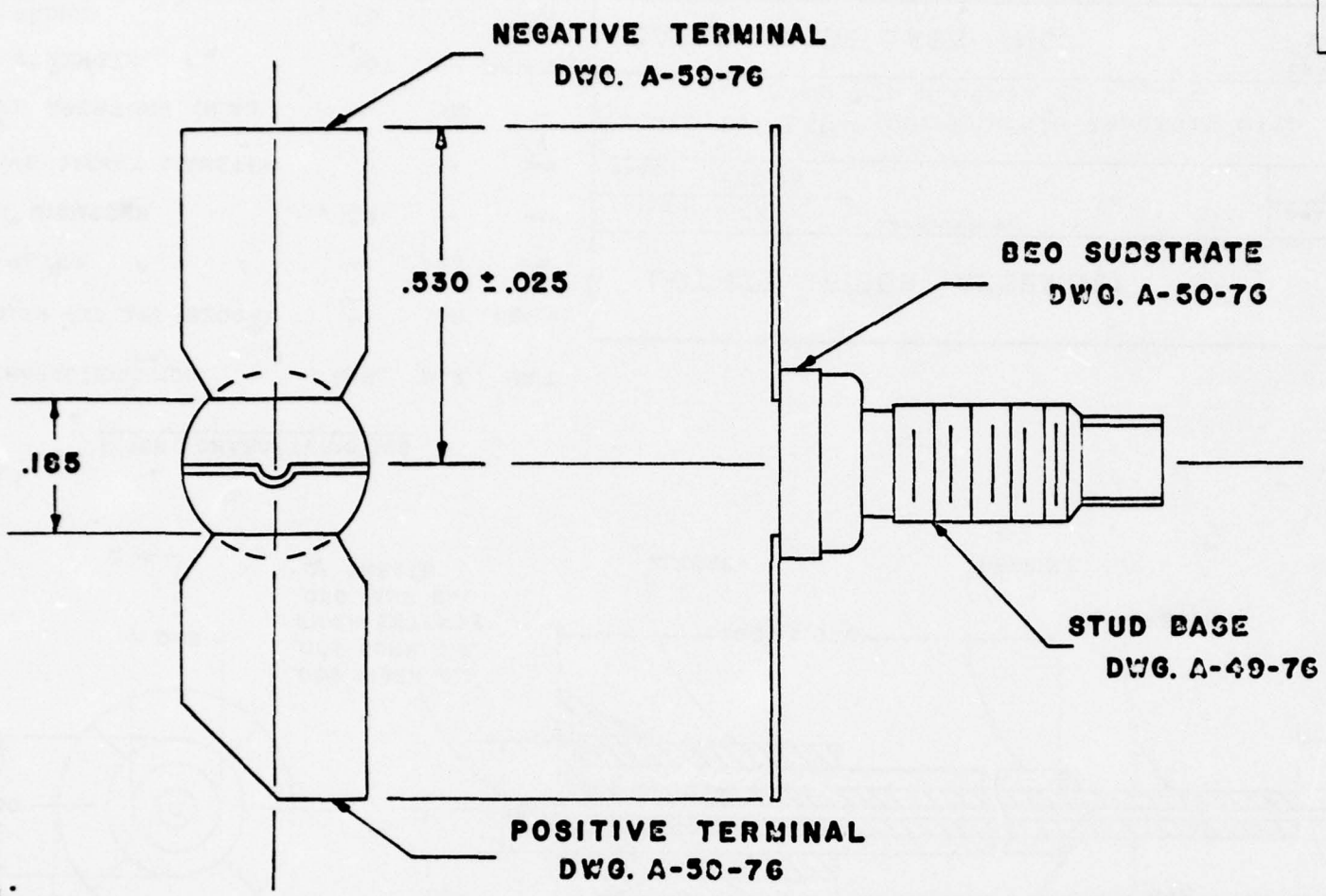
LDT 177 POSITIVE TERMINAL		
SCALE:	APPROVED BY	DRAWN BY M.R.
DATE: 12-10-76		
Figure 15. LED Electrode (POS.).		
LASER DIODE LABS. INC.		DRAWING NUMBER A-50-73



MATERIAL - KOVAR

TOL.± .002

LDT 177 NEGATIVE TERMINAL		
SCALE:	APPROVED BY	DRAWN BY M.R.
DATE: 12-10-76		
Figure 16. LED Electrode (NEG.).		
LASER DIODE LABS. INC.		DRAWING NUMBER A-50-76

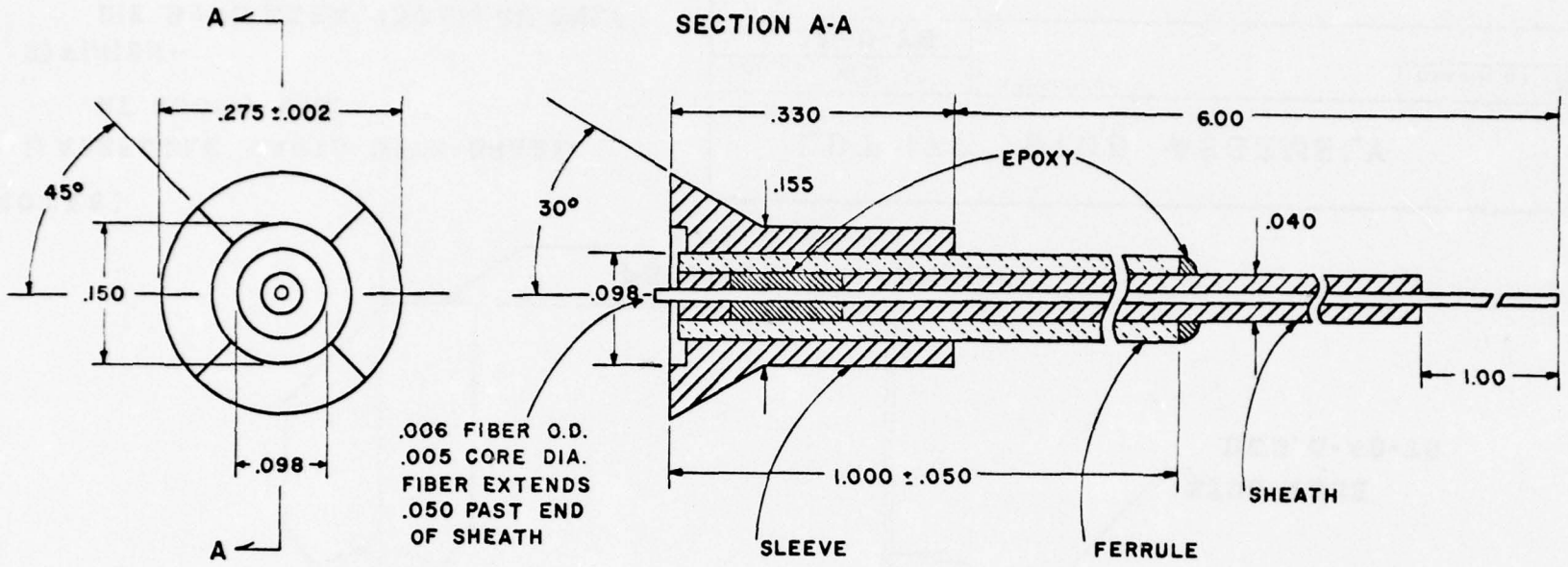


NOTES:

1) ASSEMBLE PARTS WITH BRAZE AT 600° C MIN.

2) FINISH –
DIE BOND AREA, 150 µin. AU ONLY
STUD, 150 µin. NI, IMMERSION AU
LEADS, 80 µin. AU

LDT 177 STUD ASSEMBLY		
SCALE: 4X	APPROVED BY	DRAWN BY M.R.
DATE: 12-10-76		
Figure 17. LED Stud Assembly.		
LASER DIODE LABS. INC.		DRAWING NUMBER A-49-76



FIBER CHARACTERISTICS

CHARACTERISTICS	MIN.	MAX.	UNIT
ATTENUATION (AT λP) (8200Å)	–	50	db/km
CORE DIAMETER	–	125	um
CLADDING DIAMETER	150	–	um
PROTECTIVE JACKET DIAMETER	1	–	mm
NUMERICAL APERTURE (N.A.)	–	0.3	–
TENSILE STRENGTH	50	–	NEWTONS
BENDING RADIUS	1.5	–	mm

LDT 177 FIBER ASSEMBLY

SCALE: 10X	APPROVED BY	DRAWN BY
DATE: 11-23-76		M.R.

Figure 18. LED Fiber-Ferrule Assembly with Support Sleeve.

LASER DIODE LABS. INC.

DRAWING NUMBER C-51-76

have not yet been determined. The LED chip is first soldered with Indium in the semicircular area of the BeO substrate. An ultrasonic gold wire bond connection is then made between the n-side of the LED chip and the negative terminal of the package.

Fiber alignment and attachment is accomplished using the apparatus shown schematically in Figure 19.

(a) The LED assembly is first secured rigidly in the diode mount and the appropriate electrical connections made to the stripline leads. The ferrule is clamped in the micromanipulator and the support sleeve placed in position on the diode end of the ferrule. The output end of the fiber is directed toward the PIN diode detector. The assembly apparatus is positioned beneath a Bausch & Lomb stereo microscope so that the LED fiber well and the fiber end are both clearly visible in the field of view.

(b) A small drop of Dow Corning Type R-6104 gel is then applied to the fiber well and is kept in place by capillary forces. The gel serves to protect the active emitting area of the LED chip and increases the coupling efficiency of the LED to the fiber by index matching. Because the gel does not completely solidify, stress induced by thermal expansion of the mechanical components cannot be transferred to the diode chip.

(c) Coarse alignment of the fiber is achieved by adjusting the x-y-z positioner so that the fiber end is located as close as possible to the LED fiber well when viewed under the microscope. Finer alignment is obtained

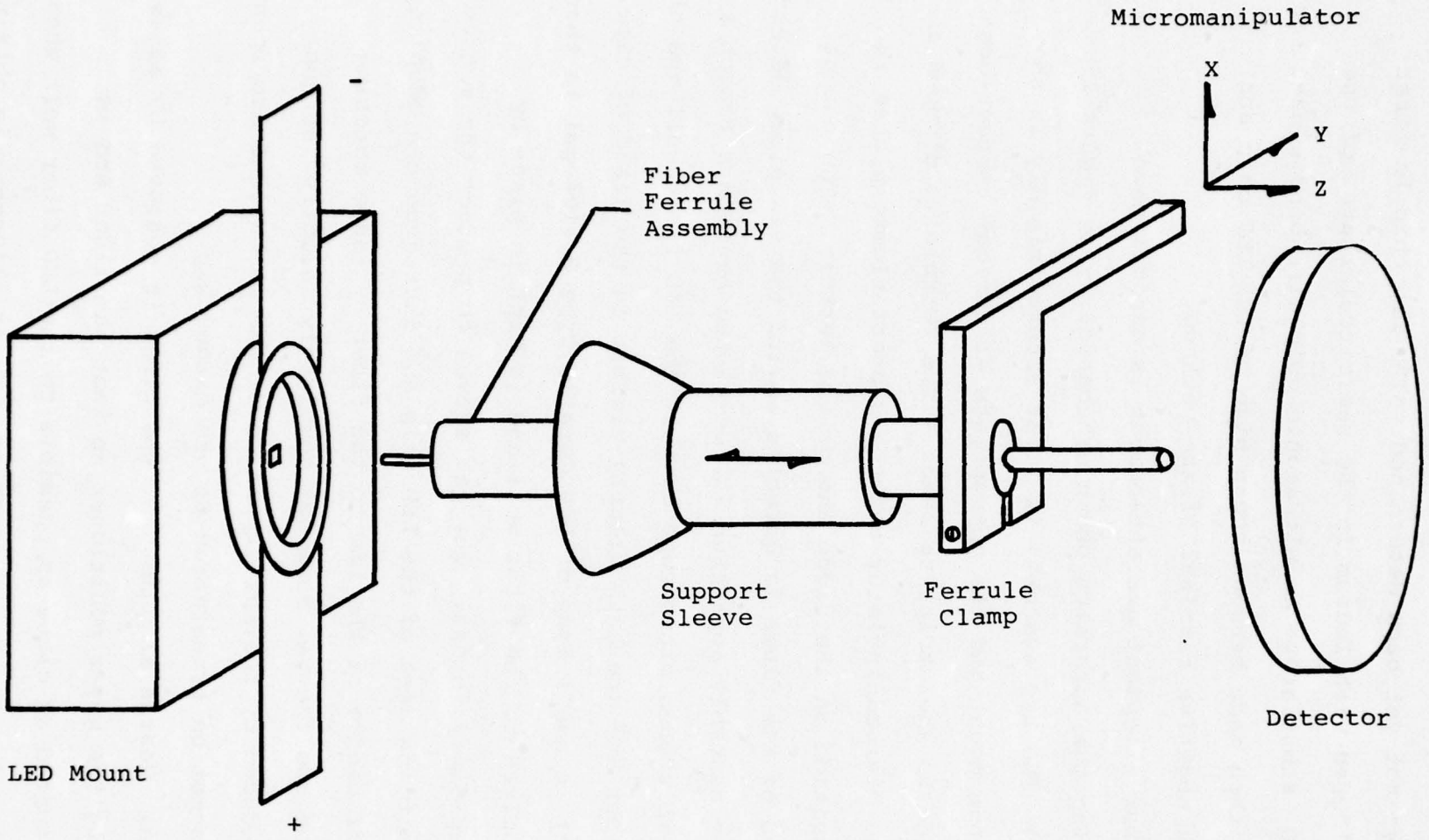


Figure 19. Schematic diagram of fiber attachment apparatus.

by adjusting to micromanipulator to peak the light emitted from the output end of the optical fiber when the LED is forward biased.

(d) After optimal alignment of the fiber-ferrule assembly with the LED chip has been accomplished, permanent attachment of the fiber to the chip carrier is made via the moveable support sleeve. The support sleeve is moved into place so that its mating face is bonded to the LED chip carrier. Epoxy is then applied between the opposite end of the support sleeve and the exposed portion of the ferrule. After the epoxy is cured, the ferrule clamp is removed and the completed LED assembly is demounted from the alignment jig. Figure 20 shows an exploded view of the LED components along with a completed unit.

3.3 Device Evaluation and Testing.

Two categories of test equipment are required for this program. The first is for lifetest/burn-in and comprises a suitable overall power supply and a number of individual current limiters. The second is for specification testing and is considerably more complex. The diversity of the tests to be performed requires an array of standard commercial test equipment along with special purpose drivers, sensors, and fixtures specific to the task at hand.

Each burn-in rack position consists of a simple DC current source to drive its LED at 100mA. A sufficient

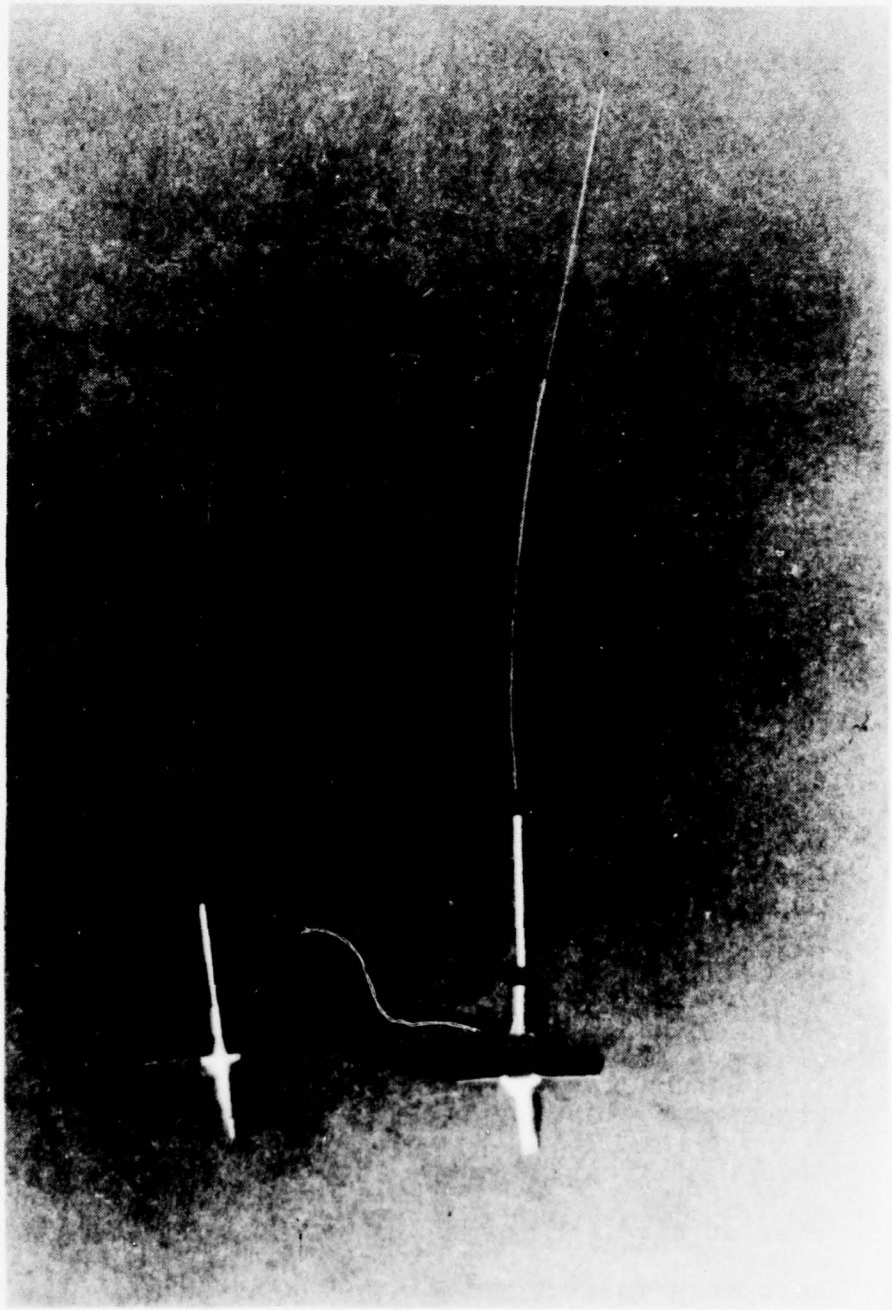


Figure 20. Photograph of Completed LED Assembly.

number of these positions, together with a power supply mounted in a standard enclosure, form a 'burn-in rack'. Specification tests may be grouped according to measurements which are made with similar equipment setups. One group of tests is power related: optical power, radiant intensity, and numerical aperture all are steady-state tests using a DC driver and DC detector. For radiant intensity, a fixed aperture and distance on the detector is needed and numerical aperture requires a slit on the detector along with a goniometer to measure angular displacement. Another group of related measurements are those associated with bandwidth: Risetime and falltime as well as baseband bandwidth require a fast high sensitivity detector and a wideband oscilloscope. The risetime and falltime test requires a fast edge pulser, where the bandwidth test calls for a wideband sinewave driver. Measuring linearity requires the same equipment as the bandwidth test and in addition requires a spectrum analyzer. A further group of related tests deal with optical wavelength. Measurement of peak wavelength requires the same DC driver as the power measurement and a spectrometer. Spectral width may be measured in the same manner as peak wavelength. The same spectrometer is needed to measure thermal impedance along with the DC driver and the fast edge pulse driver. Also, a variable temperature test head must be used. The remaining tests are forward and reverse voltage, and

TABLE 4. Communications LED Test Equipment Requirements.

Specification Tests	Test Equipment: 1 Variable Temp. Head	2 D.C. Driver Square Wave Driver	3a Pulse Driver Low Distortion Sine Wave Gen.	3b Var. Frequency Sine Wave Gen.	4a Curve Tracer	4b CW Detector Wideband Detector	5 Wideband Scope Spectrum Analyzer	6 Spectrometer	7	8	9	10		Notes:
λ_p		X										X		1.
V_f							X							
V_r							X							
P_{opt}		X						X						
$\Delta\lambda$		X										X		1.
N.A.		X						X						2.
$T_{r,f}$			X						X	X				
t_s	X	X		X					X	X		X		
Lin.					X				X	X	X			
I		X						X						3.
B_{Hz}						X			X	X				

Notes:
1. Peak wavelength, λ_p, and spectral width $\Delta\lambda$, may be consolidated.
2. Measurement performed with aperture, detector, and goniometer.
3. Measurement performed with circular aperture on detector.

these may be measured via standard techniques. Throughout specification testing, special fixtures designed to connect to and heatsink the diode under test will be used as required.

Choices for the various standard equipments to be employed are being made and attention is being given to overall system design as well as the design of special test fixtures and their subassemblies to be used for specification testing. The matrix for test equipment requirements is shown in Table 4.

3.4 Production Engineering.

The preliminary manufacturing sequence for the mass production of etched-well LED's for fiber optic communication is shown in the flow chart of Figure 21. In addition, estimates of minimum man-hour requirements for the fabrication of the communications LED at a rate consistant with the production of 500 units per week are tabulated in Table 5.

SECTION IV

SUMMARY AND CONCLUSION

The first quarter of the program has witnessed completion of the package design phase, and more significantly, finalization of processing techniques for wafer fabrication of the etched well light emitting diode has been successfully accomplished. Procurement of the low inductance stripline stud mount for the LED has been completed but, to date, little success in obtaining

Figure 21. Flow Chart of Manufacturing Process for Etched Well Light Emitting Diode.

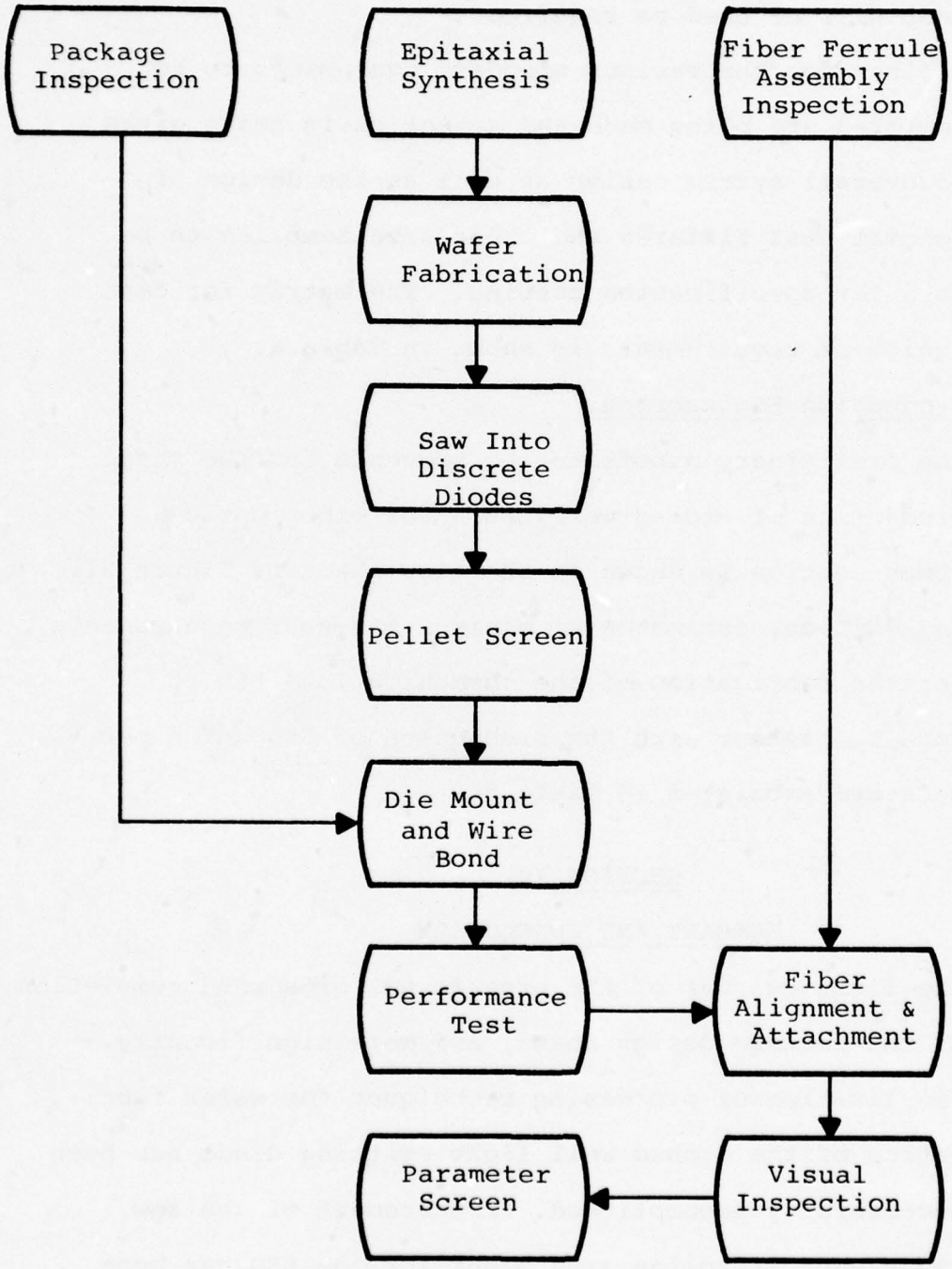


TABLE 5.

Minimum Man Hour Requirements for Fabrication of Etched Well Light Emitting Diodes.

	Manufacturing Sequence	Man Hour Requirement
1.	Epitaxial Synthesis	8.0
2.	Photolithography	5.6
3.	Metalization	1.1
4.	Well Definition	5.0
5.	Cutting	16.8
6.	Pellet Screen	1.5
7.	Diode Mounting	12.0
8.	Device Pretest	1.5
9.	Fiber Attachment	20.0
10.	Inspection	1.5

* Figures are yield adjusted for a rate of 100 units per day.

a suitable source for the fiber optic subassembly has been achieved. Because most of the effort during this quarter has been oriented toward solving some of the extremely difficult wafer processing problems, the fabrication and testing of finished engineering samples has been delayed.

Plans for the second quarter, include the fabrication, testing, and delivery of the first engineering samples and and completion of the test and evaluation facilities required to fully characterize device performance. Negotiations with potential suppliers of the optical fiber pigtail subassembly will be accelerated in order to meet the scheduled completion of the second set of engineering samples.

APPENDIX A

Engineering Man-Hour Utilization
for the First Quarter of the Program.

R. B. Gill	88 Hrs.
T. E. Stockton	176 Hrs.
A. Gennaro	65 Hrs.
S. Klunk	16 Hrs.
R. Albano	120 Hrs.
Manufacturing Personnel	524 Hrs.

APPENDIX B

BIOGRAPHIES OF KEY PERSONNEL.

Robert B. Gill

Robert Gill received the B. S. degree in physics from Fairleigh Dickinson University in 1963 and the M. S. degree in physics from Stevens Institute of Technology in 1967.

Mr. Gill was employed at RCA Laboratories in 1963, where he was primarily engaged in the development of semiconductor devices, including lead-salt infrared photoconductive and photovoltaic detectors and thin-film gallium arsenide solar cells. His responsibilities included the preparation and characterization of materials, device design and evaluation, and process development.

In 1968, Mr. Gill transferred to the Optoelectronic Products Department of the RCA Solidstate Division where he was assigned to Semiconductor Engineering. His primary responsibilities were the solution of problems associated with GaAs, (GaAl)As, and GaP single and multiple epitaxy and the design of electroluminescent devices including injection lasers and visible and infrared emitters utilizing these materials. His work in these areas contributed to the design and development of the first commercial GaAs and (GaAl)As single heterojunction and LOC injection laser and laser arrays.

In 1971, Mr. Gill joined the staff of Laser Diode Laboratories, Inc., as Operations Manager, Devices, and became the President in 1973. In this position he is in charge of R & D as well as production engineering on materials, designs and processes for the injection lasers and laser arrays.

Under his direction Laser Diode Laboratories, Inc., developed

and was the first to introduce into commercial sale:

(a) a continuous wave room temperature GaAlAs laser diode

(b) a radiation resistant, heterojunction light emitting diode

(c) a high power, high duty cycle, triple heterojunction, stacked laser array

(d) a fiber optic coupled version of the preceding device, and

(e) a 820 nm light emitting diode which was qualified for use as an infrared source in the Goggle Program.

Mr. Gill is author or co-author of 19 technical and scientific papers.

Thomas E. Stockton

Thomas Stockton was graduated with high distinction in Physics from Rutgers University where he received his Bachelor's Degree in 1971.

Mr. Stockton was employed at RCA Laboratories in 1972 where he was primarily engaged in Optoelectronic device research, design, fabrication and testing. Primarily responsible for the development of multi-heterojunction injection lasers, his assignments included crystal growth, liquid phase epitaxy, contact development, diffusion technology and all aspects of device processing and assembly. His significant achievements included development of a high power LOC laser for optical communications and fuzing, CW operation of AlGaAs multiple heterojunction lasers, degradation studies leading to improved high damage threshold semiconductor lasers, and a cold cathode electron emitter.

Mr. Stockton joined the staff at Laser Diode Laboratories, Inc., in the fall of 1974 as Operations Manager, Devices.

Among the programs concluded under his leadership, were the introduction of the first commercial room temperature continuous wave injection laser and the development of several fiber optic coupled GaAs arrays capable of emitting up to 350 watts from a .040 inch planar aperture.

He has co-authored one paper and holds a patent for a defect free liquid phase epitaxial process. Mr Stockton is a member of Phi Beta Kappa and the IEEE.

Albert Gennaro

Mr. Gennaro received the B. S. degree in physics from Fairleigh Dickinson University in 1958. From 1958 to 1960 he pursued graduate studies in physics at Stevens Institute of Technology.

From 1960 to 1962 Mr. Gennaro was employed by the Solid State Division of Bendix Corporation where he was engaged in the design and development of transistors and diodes. In 1962 he joined the Solid State Division of RCA where he worked as a product development engineer in the development of designs and processes for the fabrication of transistors and integrated circuits. In 1972 Mr. Gennaro joined Laser Diode Laboratories as Manufacturing Manager GaAs Crystal Production. He later transferred to the device operation at Laser Diode Laboratories.

He currently is Manager, Product Development within the device operation. In his current capacity, Mr. Gennaro is responsible for device design and the development of processes required for the fabrication of heterojunction LED's suitable for use as sources in high speed communication applications.

In addition, Mr. Gennaro is responsible for the design and fabrication of all fiber optic coupled light emitting diodes, laser diodes and laser array package assemblies.

Steven Klunk

Steven Klunk received the A.A. Diploma in Engineering Technology from Cleveland Institute of Electronics in 1969 and has attended the University of Maryland.

From 1961-1967, Mr. Klunk was with the U.S.A.F. where he was engaged in photographic systems repair and maintainance.

In 1967, he joined Perkin Elmer Corp where he worked as a field engineer on HF systems. From 1969 to 1972 Mr. Klunk was with the Applications Group of RCA's Optoelectronic Products Activity. At RCA his primary responsibilities included the design and fabrication of laser modulators, and burn-in and life test equipment for support of that activity's injection laser product development effort.

Mr. Klunk joined Laser Diode Laboratories, in 1972 as an applications engineer. In this capacity he has been responsible for the design and fabrication of special laser diode modulators, test equipment and laser illuminator systems. He is currently engaged in the development of LDL products intended for use in the modulation of room temperature CW laser diode at rate ranging from 10 to 500 Megahertz.

Mr. Klunk has co-authored two technical papers on modulators and modulator design for pulsed operation of laser diodes.

Robin Adair

Mr. Adair earned his B.S. EE degree at New Jersey Institute of Technology, graduating Cum Laude in 1975. His senior project won awards from both NJIT and the IEEE, and was published by the IEEE.

He joined Laser Diode Laboratories in 1976 as an Applications Engineer and is responsible for design and fabrication of electronic support and test equipment for semiconductor diode lasers. He is currently developing burn-in, test, and modulator circuits for both high duty cycle lasers and high radiance communications LED's.

APPENDIX C

ELECTRONICS COMMAND
TECHNICAL REQUIREMENTS

SCS-511
14 AUG 1975

LIGHT EMITTING DIODE FOR USE IN FIBER OPTIC COMMUNICATIONS

1. SCOPE

1.1 Scope.- This specification covers the detail requirements for Gallium Aluminum Arsenide (GaAlAs) light emitting diode (LED) devices having a wavelength of 820 nanometers (nm), compatible with fiber optic cables and systems employing the use of fiber optics.

1.2 Maximum operating conditions:-

I_F = 150 mA

V_r = 3.0 V

I_r = 10 μA

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on the date of invitation for bids or request for proposals, forms a part of this specification to the extent specified herein:

SPECIFICATION

MILITARY

MIL-S-19500 Semiconductor Devices, General Specification for.

STANDARDS

MILITARY

MIL-STD-202 Test Methods for Electronic and Electrical Component Parts

MIL-STD-750 Test Methods for Semiconductor Devices.

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer. Both title and number or symbol should be stipulated when requesting copies.)

2.2 Other publications.- The following documents form a part of this specification to the extent specified herein. Unless otherwise indicated, the issue in effect on date of invitation for bids or request for proposal shall apply.

Laser Parameter Measurements Handbook, by H. G. Heard.

(Application for copies should be addressed to John Wiley & Sons, Inc., New York, N.Y.)

3. REQUIREMENTS

3.1 General description.- The LED devices are heterojunction devices used at a high data rate at a wavelength compatible for fiber optic cables. The device shall have an optical output and be optimized for a wavelength of 820 nm. fiber

3.2 Performance characteristics.- Performance characteristics shall be as specified in Tables III, IV and V and as follows:

3.2.1 Radiant intensity.- Radiant intensity of the unit, prior to the attachment of the optical fiber, shall be a minimum of 2 mW/Sr (See 4.6.3).

3.2.2 Linear source size.- The linear source size of the unit, prior to the attachment of the optical fiber, shall be a minimum of 50 µm and a maximum of 55 µm. (See 4.6.2).

3.2.3 Process conditioning.- All units shall be process conditioned. (See Table I and 4.5.1).

3.2.4 Linearity.- With a fundamental of 1 MHz the second harmonic shall be at least 35 db down from the fundamental.

3.2.5 Burn-in.- All units shall be burned-in. (See 4.5.2).

3.3 Design, construction and physical dimensions.- The design, construction and physical dimensions shall be as specified in Figure 1 and herein.

3.3.1 Lead material and finish.- Lead material shall be Kovar or alloy 42 with a hot solder dip finish.

3.3.2 Metals.- External metal surfaces shall be corrosion resistant or shall be plated or treated to resist corrosion.

3.4 Marking.- Marking shall be in accordance with MIL-S-19500 except the following information shall be marked on each unit.

(a) Date code.
(b) Manufacturer's identification.
(c) Part number: SCS-511.
(d) Power output in mW at I_F = 100 mA.

3.5 Resistance to solvents.- When the device is subjected to solvents, there shall be no evidence of: (a) mechanical or electrical damage, (b) deterioration of the materials or finishes, and (c) illegibility of case marking.

3.6 Solderability.- Leads shall be solderable.

3.7 Thermal shock.- After being subjected to specified temperature cycling, there shall be no evidence of defects or damage to case, leads, or seals or loss of marking legibility.

3.8 Shock.- After being subjected to a shock of 500g for .5 msec, there shall be no evidence of defects or damage to leads or seals. Also, the device shall be electrically operable (see Subgroup 2 of Table III).

3.9 Vibration fatigue.- After being subjected to a vibration with a constant peak acceleration of 20g minimum and a frequency of 60 ± 20 Hz for at least 32 ± 8 hours, there shall be no evidence of defects or damage to case, leads or seals. Also, the device shall be electrically operable (see Subgroup 2 of Table III).

3.10 Vibration, variable frequency.- After being subjected to a vibration with a constant peak acceleration of 20g minimum and a frequency range between 100 and 2000 Hz, there shall be no evidence of defects or damage to case, leads, or seals. Also, the device shall be electrically operable (see Subgroup 2 of Table III).

3.11 Constant acceleration.- After being subjected to a constant acceleration of 1000g for 1 minute in each of its orientations, there shall be no evidence of defects or damage to case, leads, or seals. Also, the device shall be electrically operable (see Subgroup 2 of Table III).

3.12 High temperature life.- After being stored at 85°C for the specified time there shall be no evidence of defects or damage to case, leads or seals or loss of marking legibility. Also, the device shall be electrically operable (see Subgroup 2 of Table III).

3.13 Steady state operation.- After being subjected to steady state operation (I_F = 100 mA) for the specified temperature and time, the device shall be electrically operable (see Subgroup 2 of Table III).

3.14 Moisture resistance.- After being subjected to the specified humidity and temperature cycling, there shall be no evidence of corrosion of external metal surfaces. Also, the device shall be electrically operable (see Subgroup 2 of Table III).

4. QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for inspection.- Unless otherwise specified in the contract, the contractor is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified in the contract, the contractor may use his own or any other facilities suitable for the performance of the inspection requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements.

4.2 Classification of inspection.- Inspection shall be classified as follows:

(a) First article inspection (does not include preparation for delivery). (See 4.4).
(b) Quality conformance inspection. (See 4.5).

4.3 Test plan.- The contractor prepared Government-approved test plan, as cited in the contract, shall contain:

(a) Time schedule and sequence of examinations and tests.
(b) A description of the method of test and procedures.
(c) Identification and brief description of each inspection instrument and date of most recent calibration.

4.4 First article.- Unless otherwise specified in the contract, the first article inspection shall be performed by the contractor.

4.4.1 First article units.- The contractor shall furnish 50 samples for first article inspection.

4.4.2 First article inspection.- The first article inspection shall consist of Table II and all the tests included in the Government-approved test plan (see 4.3), to show compliance with the requirements of Section 3. No failures shall be permitted.

4.4.2.1 Order of testing.- Prior to first article inspection, all units shall have been process conditioned followed by burn-in.

4.5 Quality conformance inspection.- Quality conformance inspection shall consist of the examinations and tests specified for Group A inspection (Table III), Group B inspection (Table IV), and Group C inspection (Table V). The following shall apply:

(a) Prior to performing Group A inspection, all units shall be subjected to the tests specified in paragraphs 4.5.1 and 4.5.2.
(b) If the manufacturer chooses the following option(s) for testing, the sample units that are to be used in Group C inspection shall be designated as such prior to conducting the referenced Group B tests. Moreover, the number of failed diodes to be counted for lot acceptance or rejection as a result of Group C test shall be equal to all failed diodes of the test in Group B inspection, which were predesignated for use in Group C inspection, plus any additional failures occurring during Group C testing.

(1) For subgroup 3 life test in Group C inspection, the manufacturer has the option of using all or a portion of the sample already subjected to 340 hours of Group B life testing for an additional 660 hours of testing to meet the 1,000 hour requirement.

(2) For the thermal shock (temperature cycling) test of Group C inspection, the manufacturer has the option of using all or a portion of the sample already subjected to 10 cycles of Group B thermal shock (temperature cycling) testing for an additional 15 cycles of testing to meet the 25-cycle requirement.

4.5.1 Process conditioning.- Process conditioning shall be performed on 100 percent of the units. The measurements and sequence shall be as specified in Table I.

4.5.2 Burn-in.- Burn-in shall be performed on 100 percent of the units for 168 hours minimum under the following conditions:

$T_a = 25°C$

$I_F = 100$ mA

4.5.2.1 Pre-burn-in measurements.- Prior to burn-in, measurement of the parameters listed in subgroup 2 of Table III shall be performed on 100% of the units at $T_a = 25°C$.

4.5.2.2 Post burn-in measurements.- Post burn-in measurements, listed in subgroup 2 of Table III, shall be performed within 8 hours of the removal of bias conditions (i.e. I_F, I_r) at 25°C. The values observed for each device shall not exceed the following, relative to the pre-burn-in measurements:

$\Delta P_{opt} = 1\%$

$\Delta \eta_p = 1\%$

Table I.- Process conditioning

Test	MIL-STD	Method No.	Details
High temperature life (non-operating)	750	1031	Storage temperature = 85°C Storage time = 48 hours min
Thermal shock	202	107	Test Condition A except t(high) = 85°C; t(low) = 40°C; time at temperature extremes = 15 minutes maximum
Constant acceleration	750	2006	1,000 g

Table II.- First article inspection

Test	Reqt Para	Method	No. of samples 2/ 3	5	7	10	25
Group A inspection	as specified	Table III 1/	To be performed on all units.				
Group B inspection	as specified	Table IV 1/					
Subgroup 1			X				
Subgroup 2				X			
Subgroup 3					X		
Group C inspection	as specified	Table V 1/					
Subgroup 1			X				
Subgroup 2				X			
High temperature life	3.12	Method 1031 of MIL-STD-750 T_a = 85°C for 1000 hrs				X	
Steady state operation life	3.13	Method 1026 of MIL-STD-750 T_a = 25°C for 2000 hrs 3/ I_F = 100 mA					X

1/ LTPD values do not apply for first article inspection.

2/ No. of samples specified for each column shall be subjected to all the tests of that column.

3/ After 2000 hours, the P_{opt} shall equal 0.475 mW minimum.

Table III.- Group A inspection
T_a = 25°C ± 5°C unless otherwise specified

Test	Condition	Test Method	Min	Max	Units	LTPD
Subgroup 1						7
Visual and mechanical inspection		Method 2071 of MIL-STD-750	See 3.3			
Terminal strength of optical fiber	Test Condition A	Method 2036 of MIL-STD-750	10		Newtons	
Subgroup 2						5
Peak emission wavelength	I_F = 100 mA	Para. 4.6.4	800	830	nm	
Forward voltage	I_F = 20 mA	Method 4011 of MIL-STD-750		1.9	V	
Reverse breakdown voltage	I_r = 10 µA	Method 4021 of MIL-STD-750	3.0		V	
Output optical power	I_F = 100 mA	Para. 4.6.8	0.5		mW	
Subgroup 3						5
Spectral width (3 db of intensity)	I_F = 100 mA	Para. 4.6.5	40	45	nm	
Bandwidth	I_p = ±50 mA +100 mA dc bias	Para. 4.6.7	32	44	MHz	
Numerical aperture	I_F = 100 mA	Para. 4.6.9		0.3		
Rise and fall time	I_p = 100 mA +5 mA dc bias 50 ohm system	Para. 4.6.6	10	20	ns	
Thermal impedance		Para. 4.6.10		20	°C/W	
Linearity	I_p = ±50 mA +100 mA dc bias	Para. 4.6.11	See 3.2.4			

Table IV.- Group B inspection

Test	Reqt Para	MIL-STD-750 Method	Conditions	LTPD
Subgroup 1				15
Physical dimensions	3.3	2071	See Figure 1	
Subgroup 2				15
Solderability 1/	3.6	2026		
Thermal shock (temperature cycling)	3.7	1051	Test Condition A except t(high) = 85°C; t(low) = -40°C 10 cycles; time at temperature extreme - 15 minutes maximum	
Moisture resistance	3.3.2,	1021		
End point measurements: Subgroup 2 of Table III	3.14			
Subgroup 3				15
Shock	3.8	2016	Non-operating, 500 g .5 ms	
Vibration fatigue	3.9	2046	Non-operating	
Vibration, variable frequency	3.10	2056	Non-operating	
Constant acceleration	3.11	2006	force applied = 1,000 g	
End point measurements: Subgroup 2 of Table III				
Subgroup 4				7
High temperature life (non-operating) See 4.5(b)	3.12	1032	T_a = 85°C	
End point measurements: Subgroup 2 of Table III				
Subgroup 5				5
Steady state operation life	3.13	1027	I_F = 100 mA at 25°C	
End point measurements: Subgroup 2 of Table III				

1/ All devices must have been through the temperature/time exposure in burn-in. The LTPD applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.

Table V.- Group C inspection.

Test	Reqt Para	MIL-STD-750 Method	Details	LTPD
Subgroup 1				15
Thermal shock (temperature cycling) (See 4.5(b))	3.7	1051	Test Condition A_1 except t(high) = 85°C t(low) = -40°C time at temperature extremes = 15 minutes, min; total test time = 72 hrs,max	
End point measurements: Subgroup 2 of Table III				
Subgroup 2				
Resistance to solvents (See 4.6.1)	3.5	Method 215 of MIL-STD-202		3 devices (no failures)
End point measurements: Subgroup 2 of Table III				
Subgroup 3				7
High temperature life (non-operating) (See 4.5(b))	3.12	1031	T_a = 85°C for 1000 hours	
End point measurements: Subgroup 2 of Table III				
Subgroup 4				
Steady state operation life	3.13	1026	I_F = 100 mA T_a = 25°C for 2,000 hours	25 devices (no failures)
End point measurements: Subgroup 2 of Table III				

1/ Limits of subgroup 2 Table III same except: P_{opt} = .475 mW minimum.

4.6 Test methods and conditions.- Conditions and methods of examination and test shall be as specified in Tables I, II, III, IV and V and as follows:

4.6.1 Resistance to solvents.- Resistance to solvents shall be performed in accordance with Method 215 of MIL-STD-202.

4.6.2 Linear source size.- The linear source size can be determined by using a microscope objective and a normal lens (for projection) combination with a magnification of at least 200X. The image shall be scanned in both vertical and horizontal directions with a calibrated silicon photodiode detector (See 6.5) masked with a 0.5 mm slit. The slit shall be positioned perpendicular to the direction scanned. The relative intensity shall be measured until it falls to 90% of its peak value. These boundaries will define the linear source size. (See Figure 2).

4.6.3 Radiant intensity (I).- The unit (driven at I_F = 100 mA) is placed a distance of approximately 1.58 centimeters from a calibrated silicon photodiode detector which is masked to a circular area (A) with a radius of 0.5 cm. The optical power output of the unit is then measured and the radiant intensity (see 6.2) is calculated. (See Figure 3).

4.6.4 Peak emission wavelength (λ_p).- Peak emission wavelength shall be measured using a grating spectrometer with a resolution of at least one angstrom.

4.6.5 Spectral width (3 db of intensity).- The spectral width, to its 3 db of intensity points, shall be measured using a grating spectrometer with a resolution of at least 10 Å.

4.6.6 Rise and fall time (t_r, t_f).- An input of 100 mA peak to peak, with a rise and fall time of 5 ns maximum is applied to the unit. The optical output pulse is then recorded.

4.6.7 Bandwidth.- A 100mA peak to peak RF wave with a 100 mA dc bias is applied to the input of the unit. Keeping the input drive current constant, the frequency of the input signal is varied. Measure light output with a silicon photodiode detector to locate the 3 db intensity points to determine bandwidth.

4.6.8 Optical output power (P_{opt}).- A calibrated silicon phtodiode detector shall be used to measure the optical output power of the unit. (See 6.5). The distance between the photodiode and the fiber end shall be as small as possible.

4.6.9 Numerical aperture (N.A.).- The numerical aperture of the optical fiber output shall be determined. Using a calibrated silicon photodiode detector (see 6.5) on a turntable, the detector is rotated through a half angle Θ until the relative intensity of power output falls to 90% of its peak value. (See 6.3).

4.6.10 Thermal impedance.- With the device mounted on a heat sink capable of being heated above room temperature, it is driven at a (0.1%) duty cycle to minimize self-heating effects. Measurement of peak output wavelength versus temperature from 20°C to 70°C are recorded. In order to take into account its own heating effects, unit is then operated at 100% duty cycle at 20°C with I_F = 100 mA and peak output wavelength is recorded. The voltage drop (V_D) across the driven output is then measured. (See 6.4).

4.6.11 Linearity.- With the device driven at 1 MHz, a spectrum analyzer with resolution of at least 1 KHz coupled to a silicon photodiode, shall be used to measure the second harmonic content.

5. PREPARATION FOR DELIVERY

5.1 Preservation, packaging and packing.- Units shall be prepared for delivery as specified in the contract.

6. NOTES

6.1 Abbreviations, symbols, and definitions.- The abbreviations, symbols and definitions are as follows:

λ_p	peak emission wavelength
ΔF	bandwidth
I	radiant intensity
I_F	average forward current
I_p	input peak current
I_r	reverse current
P_{opt}	optical power output
t_r	rise time
t_f	fall time
V_D	voltage drop
V_r	breakdown voltage (reverse)

6.2 Radiant intensity (I).- Radiant intensity is defined as follows:

$$I = \frac{P_\lambda}{\Omega}$$

where: P_λ is power measured by detector

Ω is the solid angle of radiation and equal to

$$2\pi \int_0^{17} \sin\theta \, d\theta$$

6.3 Numerical aperture (N.A.).- Numerical aperture is defined as

$$N.A. = \sin \theta$$

6.4 Thermal impedance (Z_t).- Thermal impedance can be calculated taking slope (α) of curve λ_p vs temperature measured in 4.6.10 and the following:

$$Z_t = \frac{\Delta T}{P}$$

where: $P = I_f V_D$

and $$T = \frac{\Delta \lambda}{\alpha}$$

where: I_f = peak input current (100 mA)

$\Delta T, \Delta \lambda$ taken from graph

6.5 Method for calibration of silicon photodiode detector.- This information can be found pages 180 to 190 in "Laser Parameter Measurements Handbook."

6.6 Fiber characteristics.- The optical fiber segments use in manufacturing the light emitting diode devices shall come from optical fiber lengths having the characteristics shown in Table VI.

Table VI.- Fiber characteristics

Characteristics	Min	Max	Unit
attenuation (at λ_p)		50	db/km
core diameter		125	um
cladding diameter	150		um
protective jacket diameter	1		mm
numerical aperture (N.A.)		0.3	
tensile strength	50		Newtons
bending radius	1.5		mm

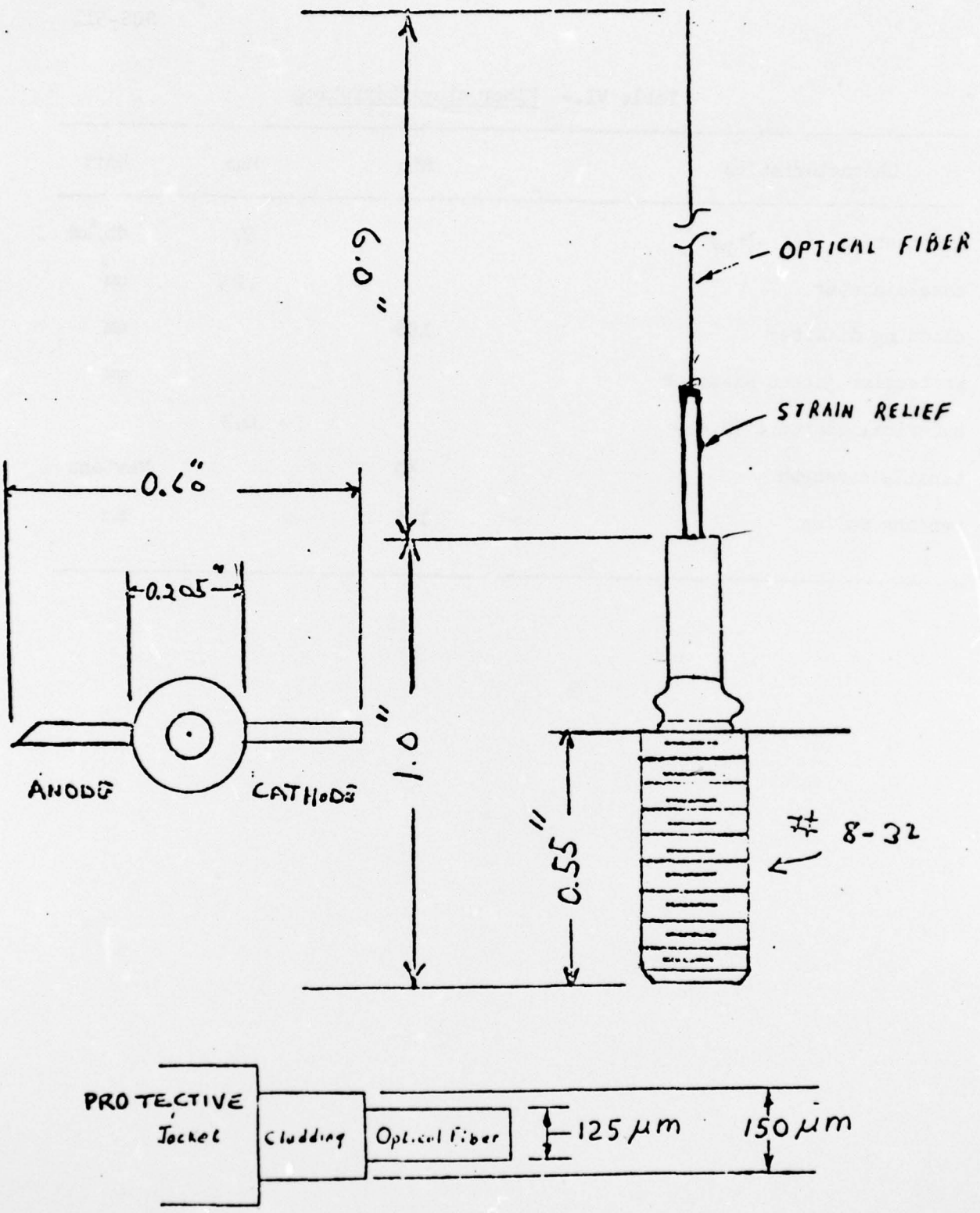
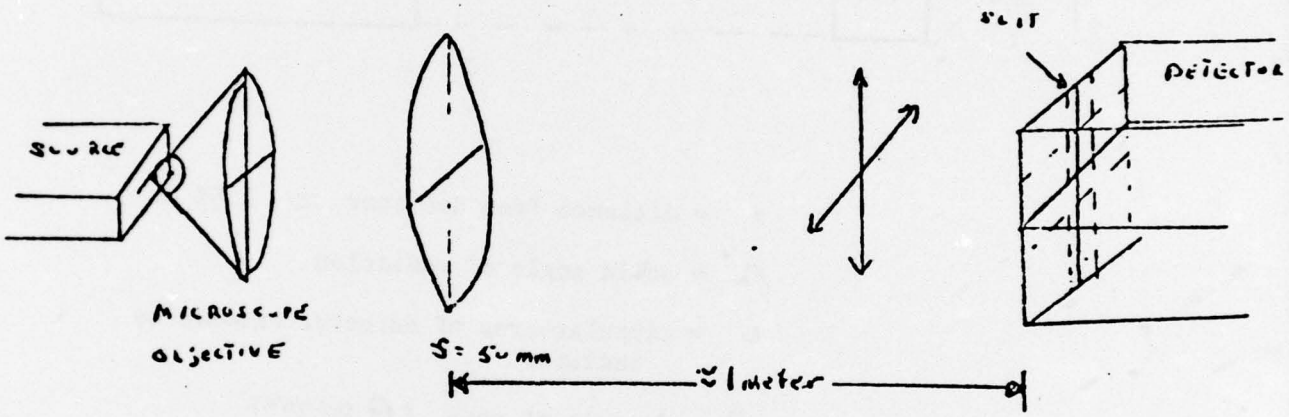
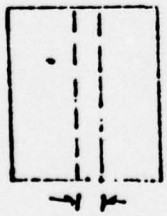


FIG. 1 PHYSICAL DIMENSIONS

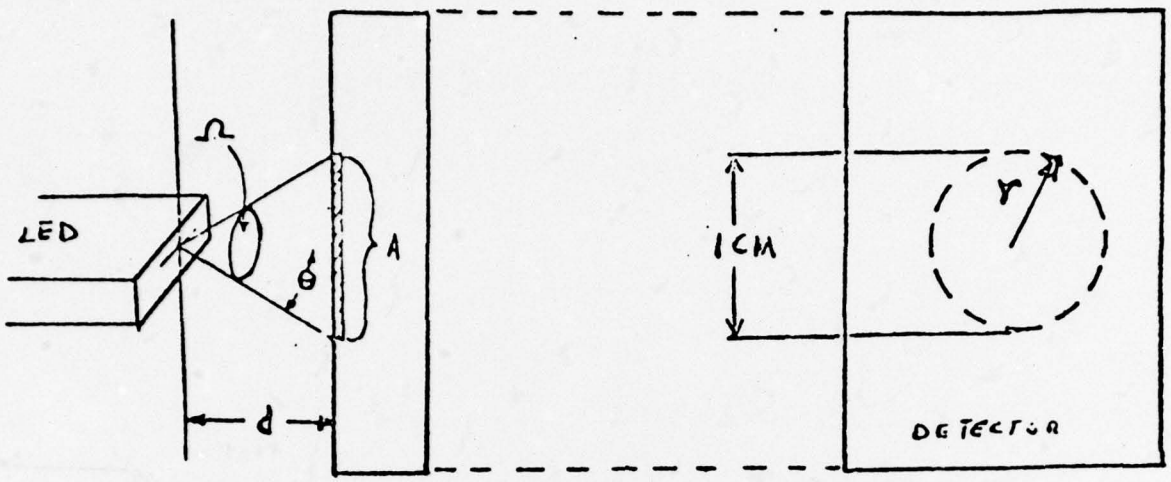


FRONT VIEW
OF DETECTOR



0.5mm = SLIT SIZE

Figure 2. [illegible]



d = distance from detector $\approx$ 1.58 cm

Ω = solid angle of radiation

A = circular area of detector exposed to radiation

θ = $\frac{1}{2}$ angle of cone ($\theta \approx 17°$)

r = radius of projection $\approx$ 0.5 cm

Figure 3 Radiant Intensity

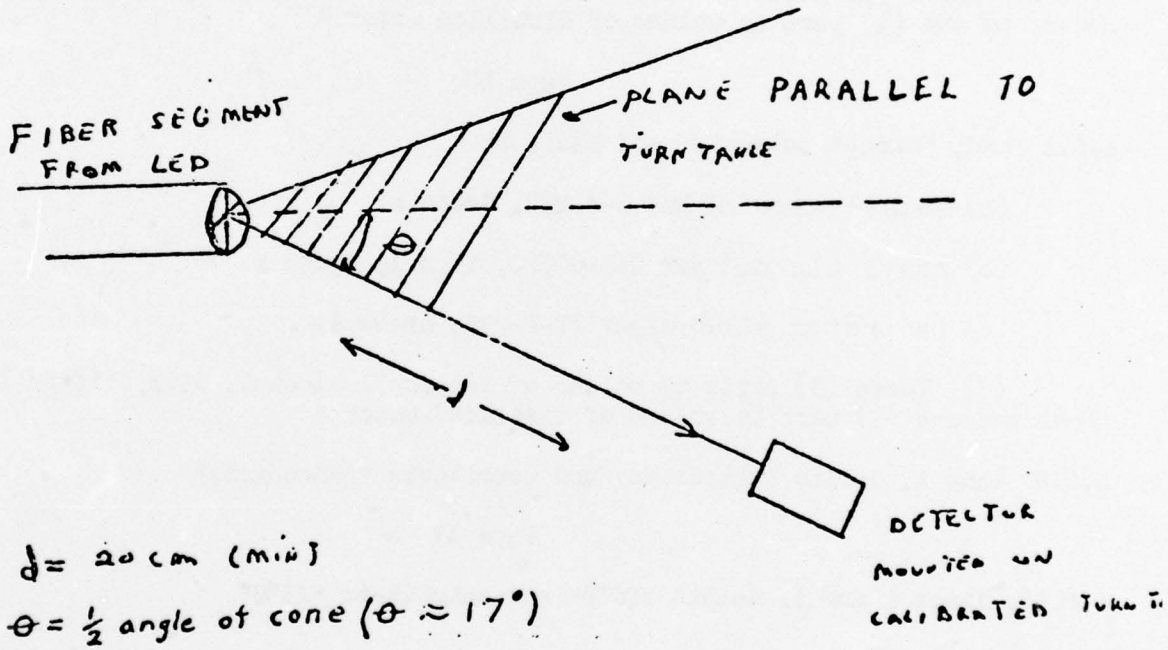


Figure 4. Numerical aperture of optical fiber output

LIGHT EMITTING DIODE FOR USE IN FIBER OPTIC COMMUNICATIONS

Page 9

Table V, Subgroup 2, under Details column for Resistance to solvents, add, "except solvents used shall be:

(a) Methyl alcohol, per O-M-232, Grade A.

(b) Ethyl alcohol, per O-E-00760, Type 1, Grade A.

(c) Isopropyl alcohol, per TT-I-735, Grade A.

(d) Three (3) parts by volume of isopropyl alcohol, as specified in (c) above and one (1) part by volume of distilled water."

Page 10

4.6.1 add, "except solvents used shall be:

(a) Methyl alcohol per O-M-232, Grade A.

(b) Ethyl alcohol per O-E-00760, Type 1, Grade A.

(c) Isopropyl alcoholper TT-I-735, Grade A.

(d) Three (3) parts by volume of isopropyl alcohol, as specified in (c) above and one (1) part by volume of distilled water."

4.6.8 line 1, delete "phtodiode" and substitute "photodiode"

Page 11

4.6.10, lines 4 and 5, delete "20°C" and substitute "25°C"

APPENDIX D

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